
EXHIBIT C



(12) **United States Patent**
Cooper et al.

(10) **Patent No.:** US 7,498,633 B2
(45) **Date of Patent:** Mar. 3, 2009

(54) **HIGH-VOLTAGE POWER SEMICONDUCTOR DEVICE**

(56) **References Cited**

(75) Inventors: **James A. Cooper**, West Lafayette, IN (US); **Asmita Saha**, Hillsboro, OR (US)

(73) Assignee: **Purdue Research Foundation**, West Lafayette, IN (US)

(*) Notice: Subject to any disclaimer, the term of this patent is extended or adjusted under 35 U.S.C. 154(b) by 0 days.

(21) Appl. No.: 11/338,007

(22) Filed: Jan. 23, 2006

(65) **Prior Publication Data**

US 2006/0192256 A1 Aug. 31, 2006

Related U.S. Application Data

(60) Provisional application No. 60/646,152, filed on Jan. 21, 2005.

(51) **Int. Cl.** **H01L 29/94** (2006.01)

(52) **U.S. Cl.** 257/341; 257/263; 257/256

(58) **Field of Classification Search** 257/256, 341, 342, 335, 339, 350, 438/142, 438/156, 176, 186, 197, 268

See application file for complete search history.

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2003/0227652 A1 * 12/2003 Ono et al. 257/341

* cited by examiner

Primary Examiner—Zandra Smith

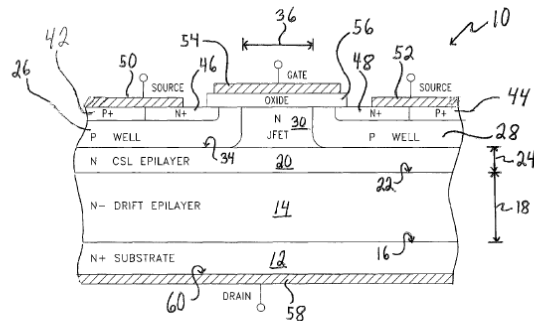
Assistant Examiner—Paul E Patton

(74) *Attorney, Agent, or Firm*—Barnes & Thornburg LLP

(57) **ABSTRACT**

A semiconductor device, such as a metal-oxide semiconductor field-effect transistor, includes a semiconductor substrate, a drift layer formed on the substrate, a first and a second source region, and a JFET region defined between the first and the second source regions. The JFET region may have a short width and/or a higher concentration of impurities than the drift layer. The semiconductor device may also include a current spreading layer formed on the drift layer. The current spreading layer may also have a higher concentration of impurities than the drift layer.

15 Claims, 4 Drawing Sheets



Title: HIGH-VOLTAGE POWER SEMICONDUCTOR DEVICE

Priority Date: Jan. 21, 2005

Filed Date: Jan. 23, 2006

Issued Date: Mar. 03, 2009

Expiration Date: Jan. 23, 2026

Inventors: James A. Cooper; Asmita Saha

Exemplary Claim: 9

Claim 9

A **double-implanted metal-oxide semiconductor field-effect transistor** comprising:

a **(SUB) silicon-carbide substrate**;

a **(DL) drift semiconductor layer** formed on a **(FS) front side** of the **(SUB) semiconductor substrate**;

a **(FS) first source region**;

a **(FSE) first source electrode** formed over the **(FS) first source region**, the **(FSE) first source electrode defining a longitudinal axis**;

a **(FBC) plurality of first base contact regions** defined in the **(d) first source region**, **(FBC) each of the plurality of first base contact regions being spaced apart from each other** in a **(FSE) direction parallel to the longitudinal axis defined by the first source electrode**;

a **(SS) second source region**;

a **(SSE) second source electrode** formed over the **(SS) second source region**, the **(SSE) second source electrode defining a longitudinal axis**;

a **(SBC) plurality of second base contact regions** defined in the **(SS) second source region**, **(SBC) each of the plurality of second base contact regions being spaced apart from each other** in a **(SSE) direction parallel to the longitudinal axis defined by the second source electrode**; and

a **(JF) JFET region defined between** the **(FS) first source region** and the **(SS) second source region**, the **(JF) JFET region having a width less than about three micrometers**.

Claim 9

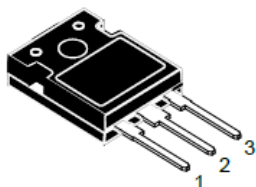
A **double-implanted metal-oxide semiconductor field-effect transistor** comprising:



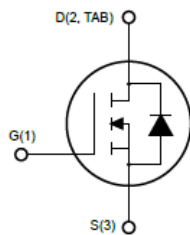
SCTW90N65G2V

Datasheet

Silicon carbide Power MOSFET 650 V, 119 A, 18 mΩ (typ., $T_J = 25^\circ\text{C}$)
in an HiP247 package



HiP247



AIM01475v1_noZen

Features

Order code	V_{DS}	$R_{DS(on)}$ max.	I_D
SCTW90N65G2V	650 V	24 mΩ	119 A

- Very high operating junction temperature capability ($T_J = 200^\circ\text{C}$)
- Very fast and robust intrinsic body diode
- Extremely low gate charge and input capacitances

Applications

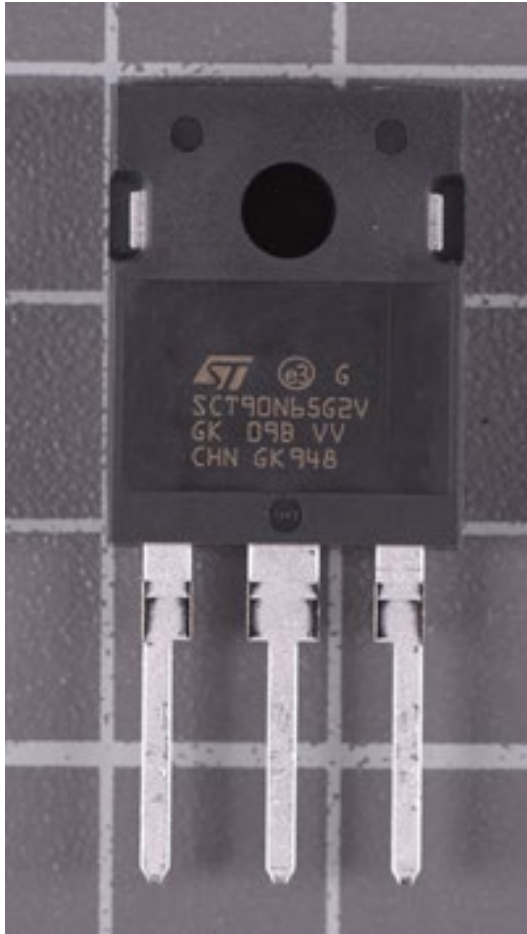
- Switching applications
- Power supply for renewable energy systems
- High frequency DC-DC converters

Description

This silicon carbide Power MOSFET device has been developed using ST's advanced and innovative 2nd generation SiC MOSFET technology. The device features remarkably low on-resistance per unit area and very good switching performance. The variation of switching loss is almost independent of junction temperature.

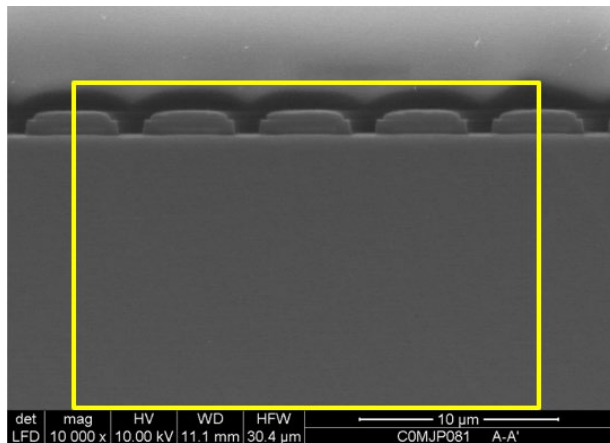
Claim 9

A **double-implanted metal-oxide semiconductor field-effect transistor** comprising:



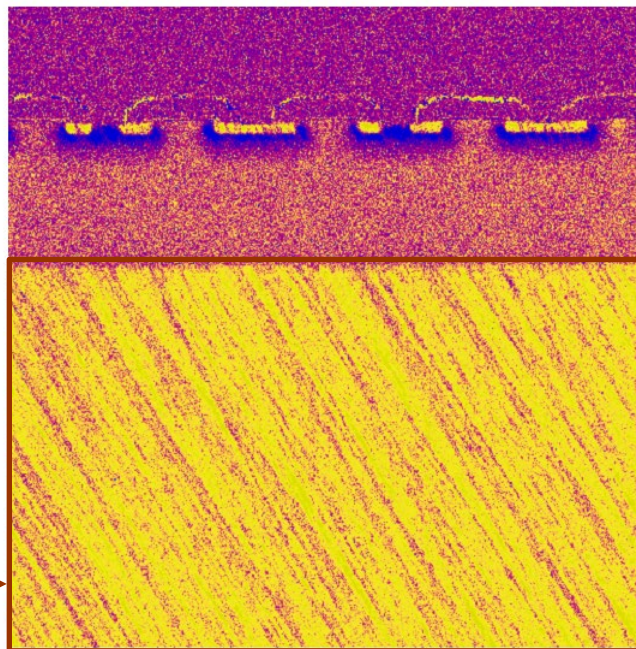
Claim 9

a **(SUB)** silicon-carbide substrate;



SEM

SUB →



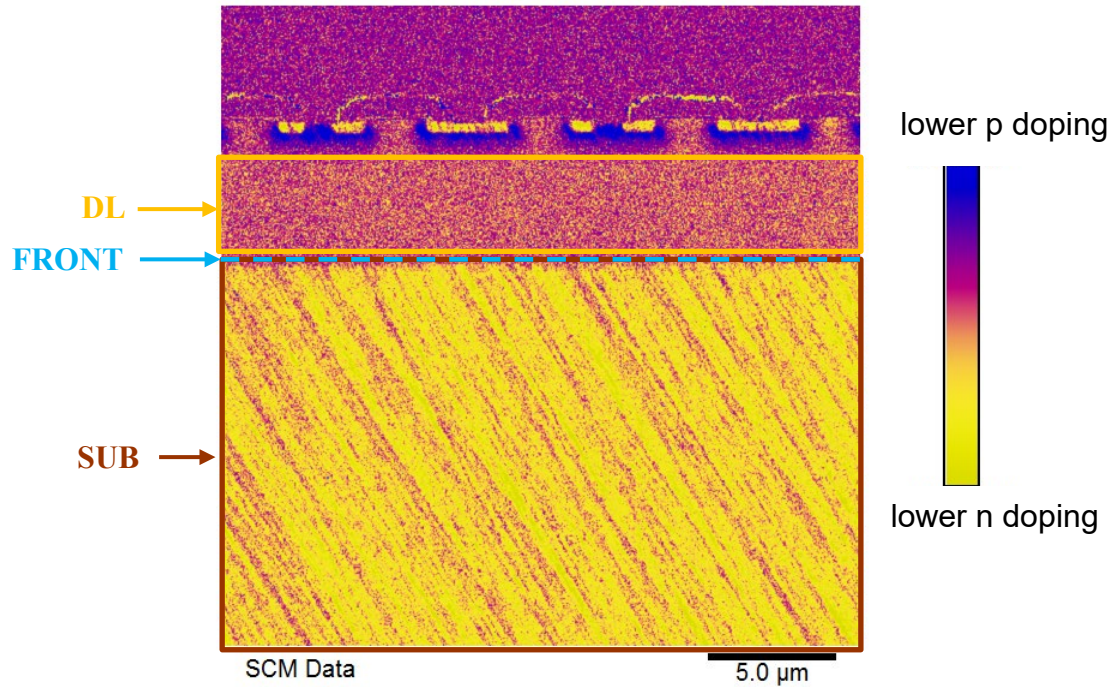
SCM Data

5.0 μm

Note: Scanning Capacitance Microscopy (SCM) taken of the framed area in the Scanning Electron Microscopy (SEM) image

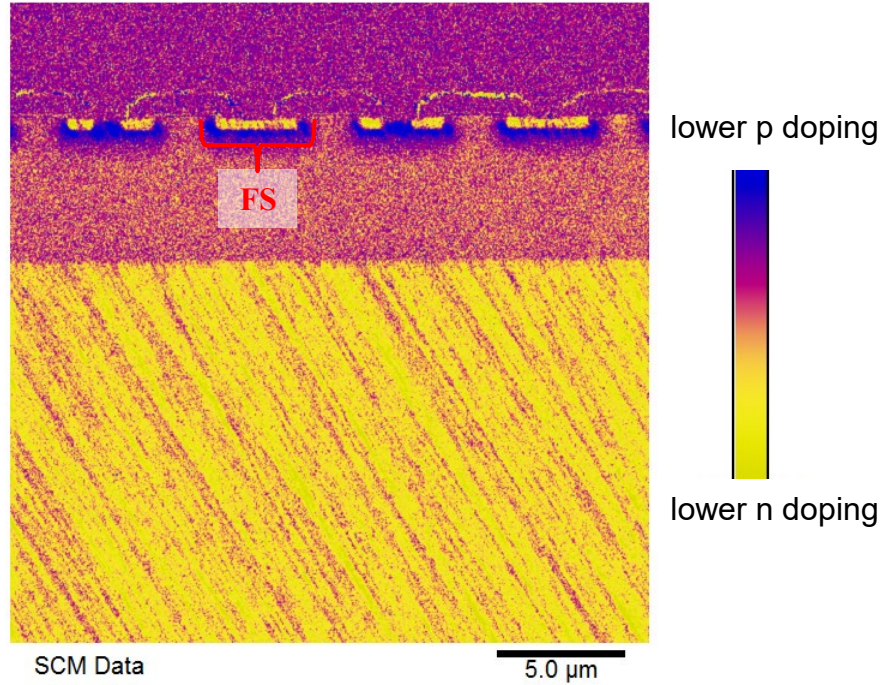
Claim 9

a **(DL)** drift semiconductor layer formed on a **(FRONT)** front side of the **(SUB)** semiconductor substrate;



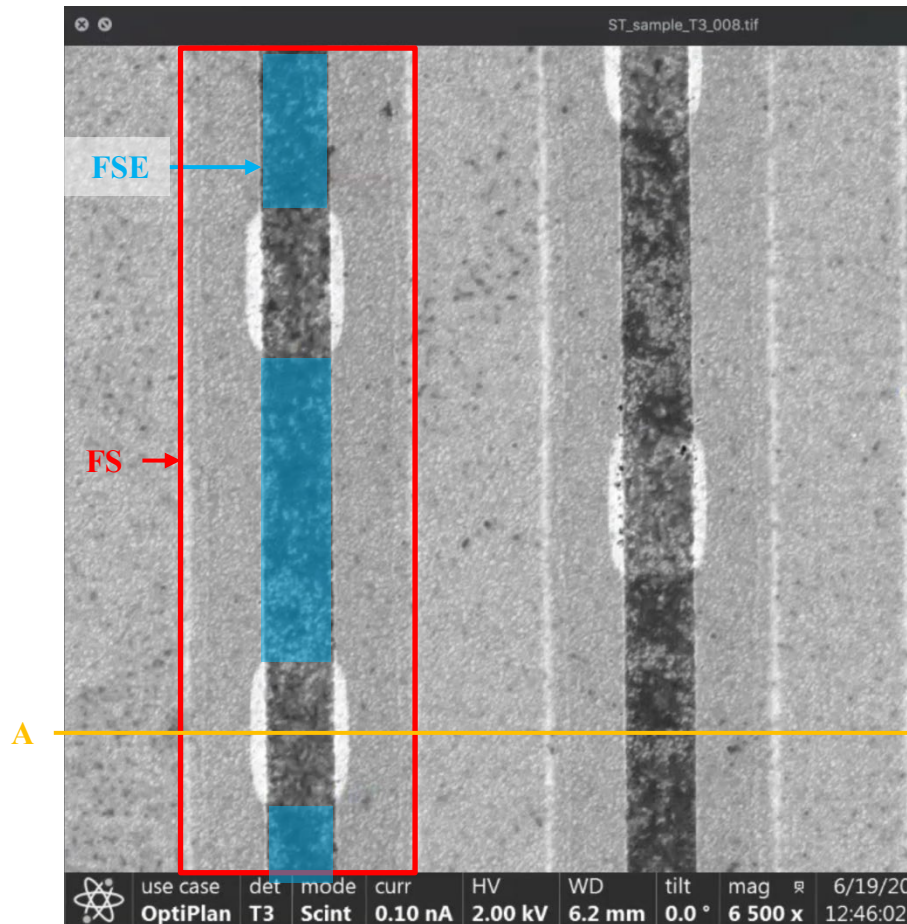
Claim 9

a **(FS) first source region;**

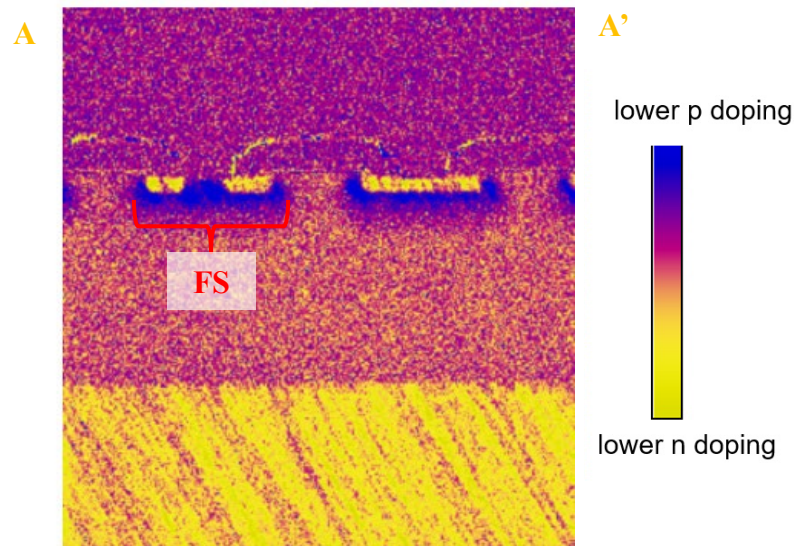


Claim 9

a (FSE) first source electrode formed over the (FS) first source region, the (FSE) first source electrode defining a longitudinal axis;



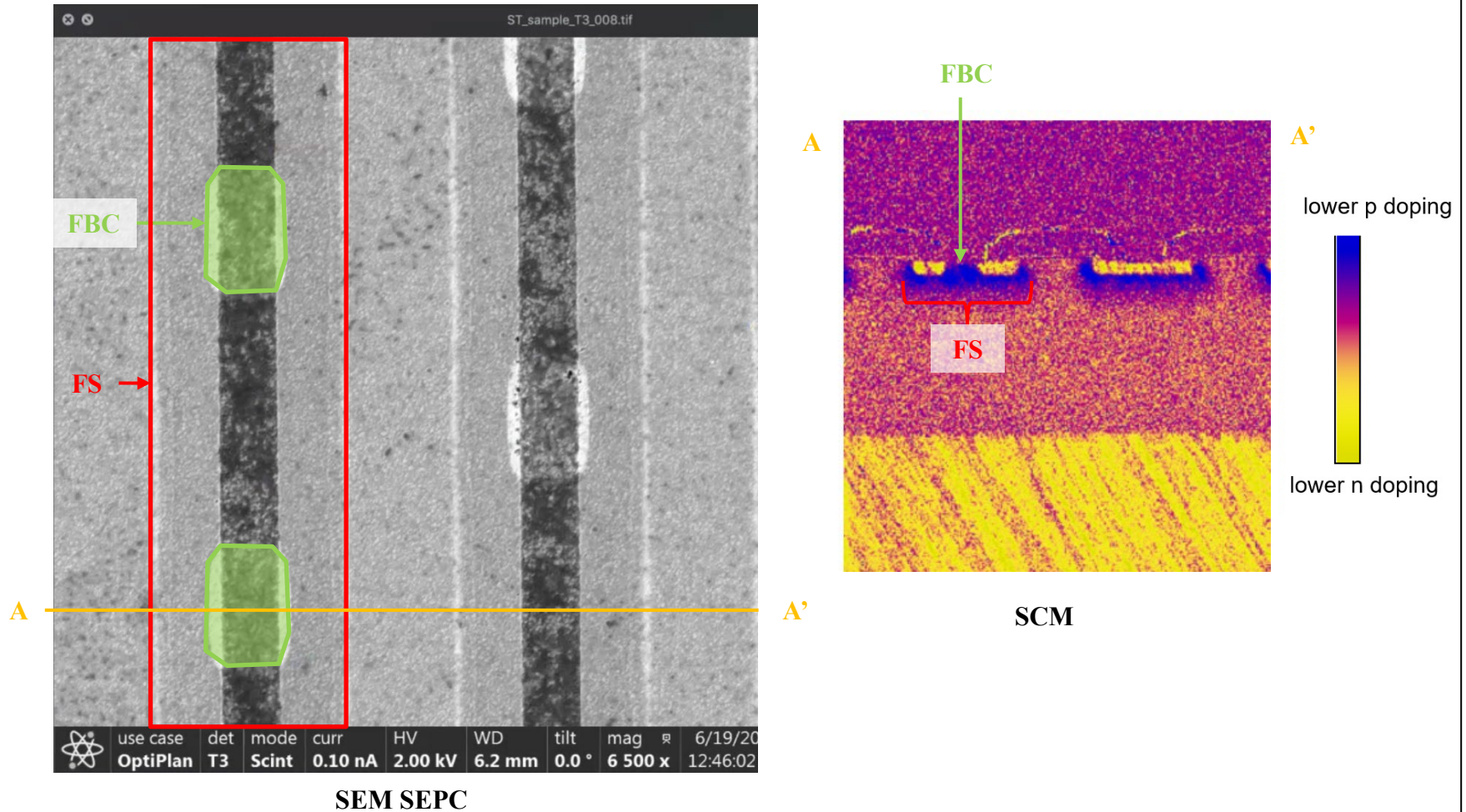
Note: Top-down view using Scanning Electron Microscopy Secondary Electron Potential Contrast (SEM SEPC), after polishing down to the silicon carbide.



Note: SCM view taken at the A-A' cross section

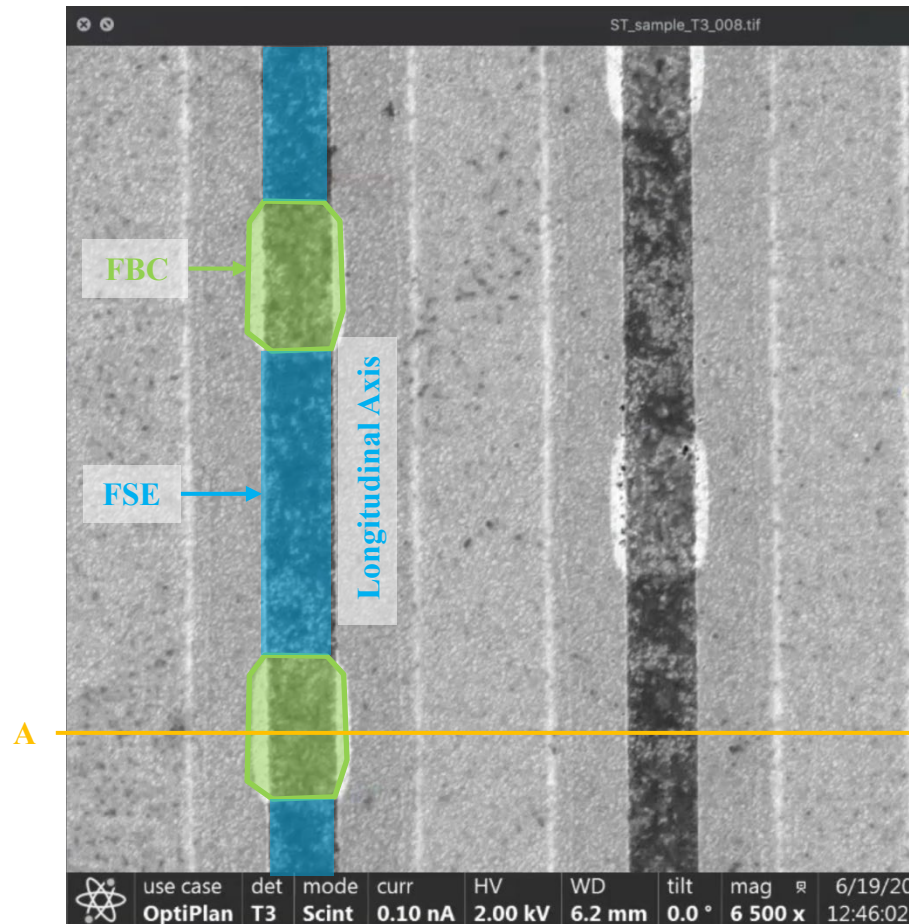
Claim 9

a (FBC) plurality of first base contact regions defined in the (FS) first source region,

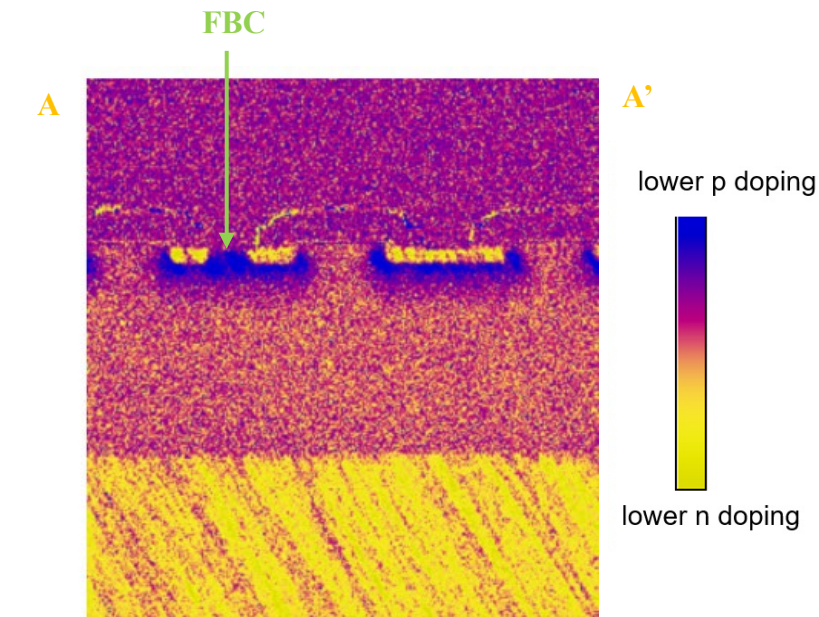


Claim 9

(FBC) each of the plurality of first base contact regions being spaced apart from each other in a (FSE) direction parallel to the longitudinal axis defined by the first source electrode;



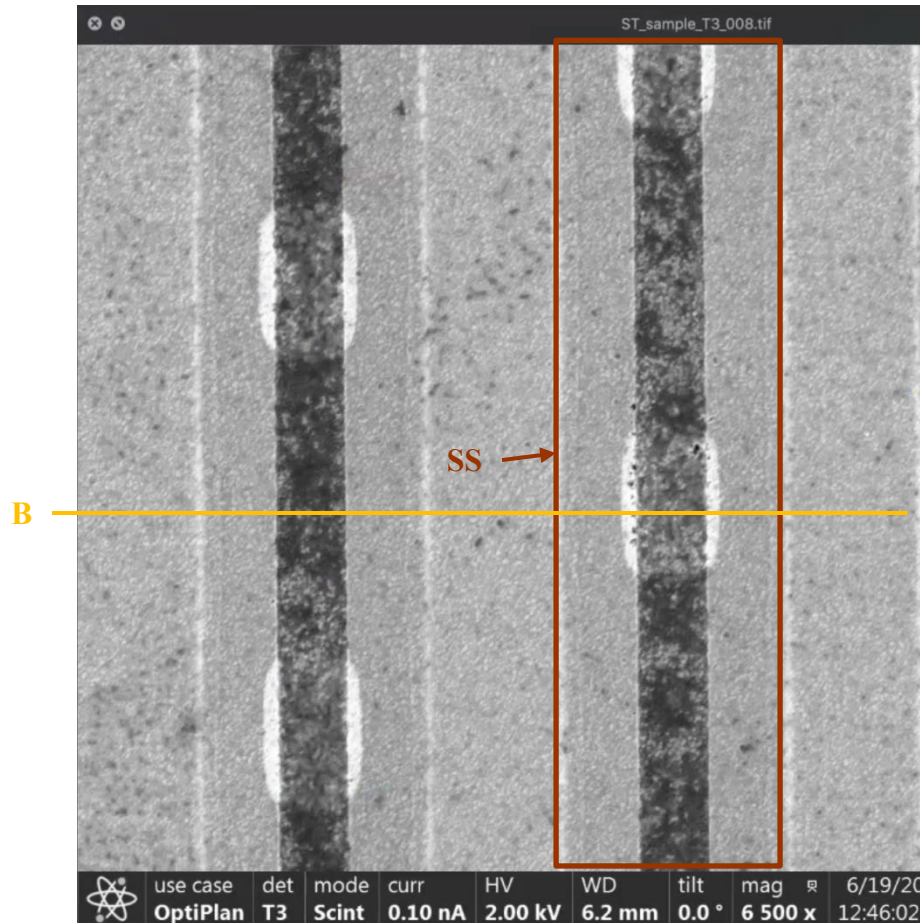
SEM SEPC



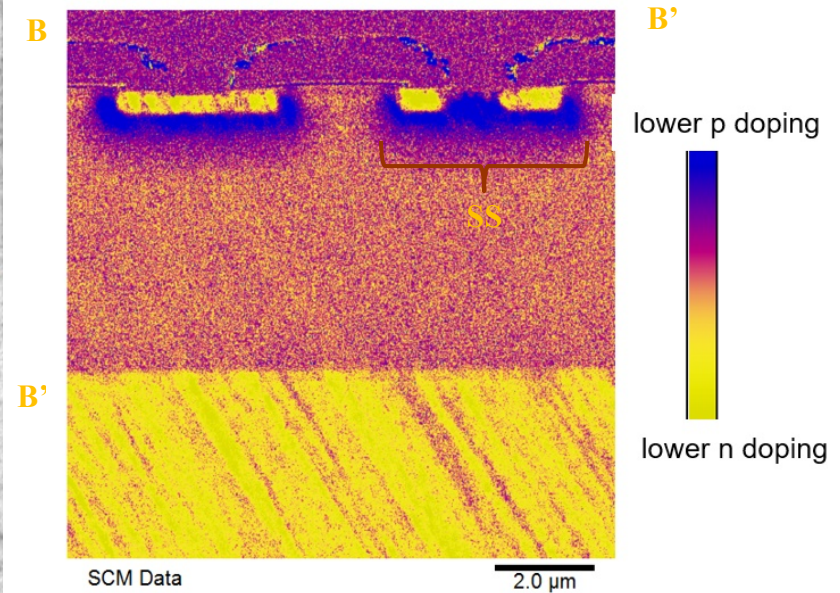
SCM

Claim 9

a (SS) second source region;



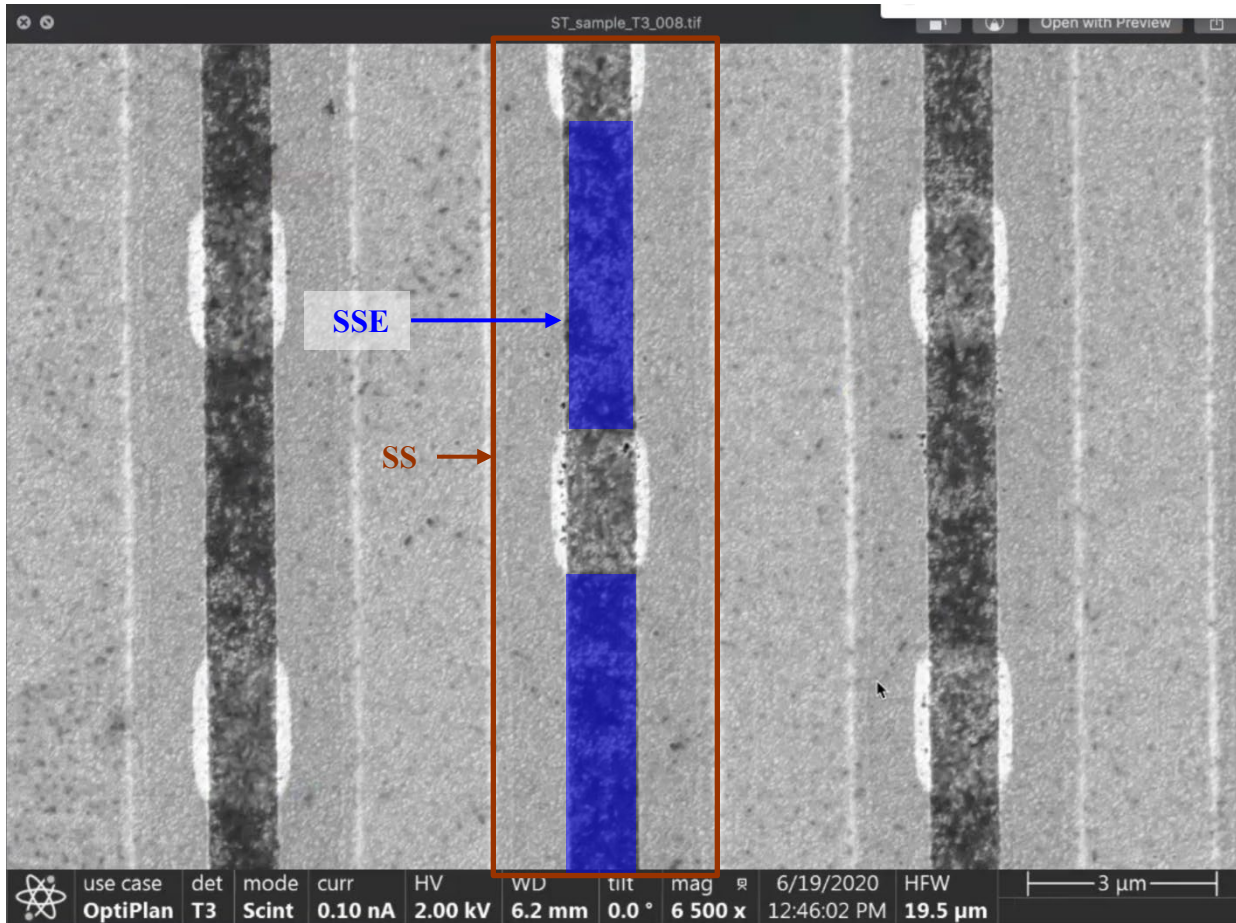
SEM SEPC



Note: SCM view taken at the B-B' cross section

Claim 9

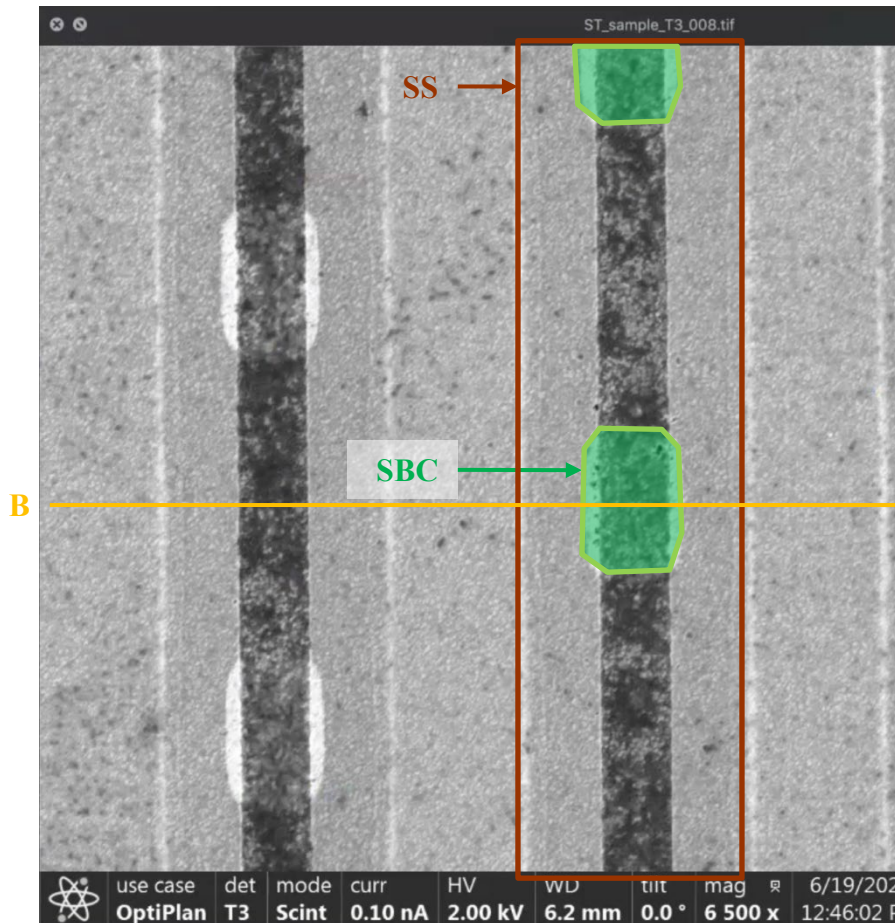
a **(SSE) second source electrode** formed over the **(SS) second source region**, the **(SSE) second source electrode defining a longitudinal axis**;



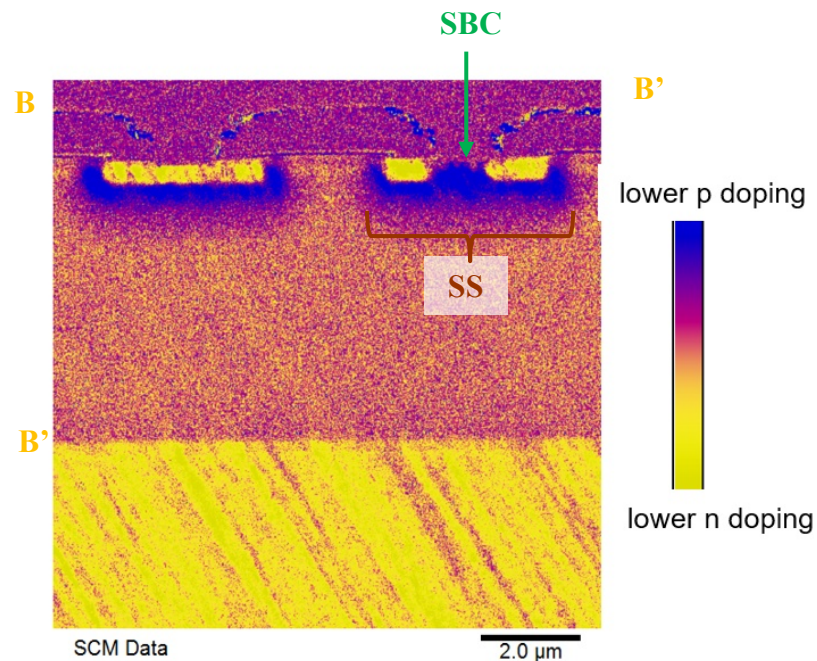
SEM SEPC

Claim 9

a (SBC) plurality of second base contact regions defined in the (SS) second source region,



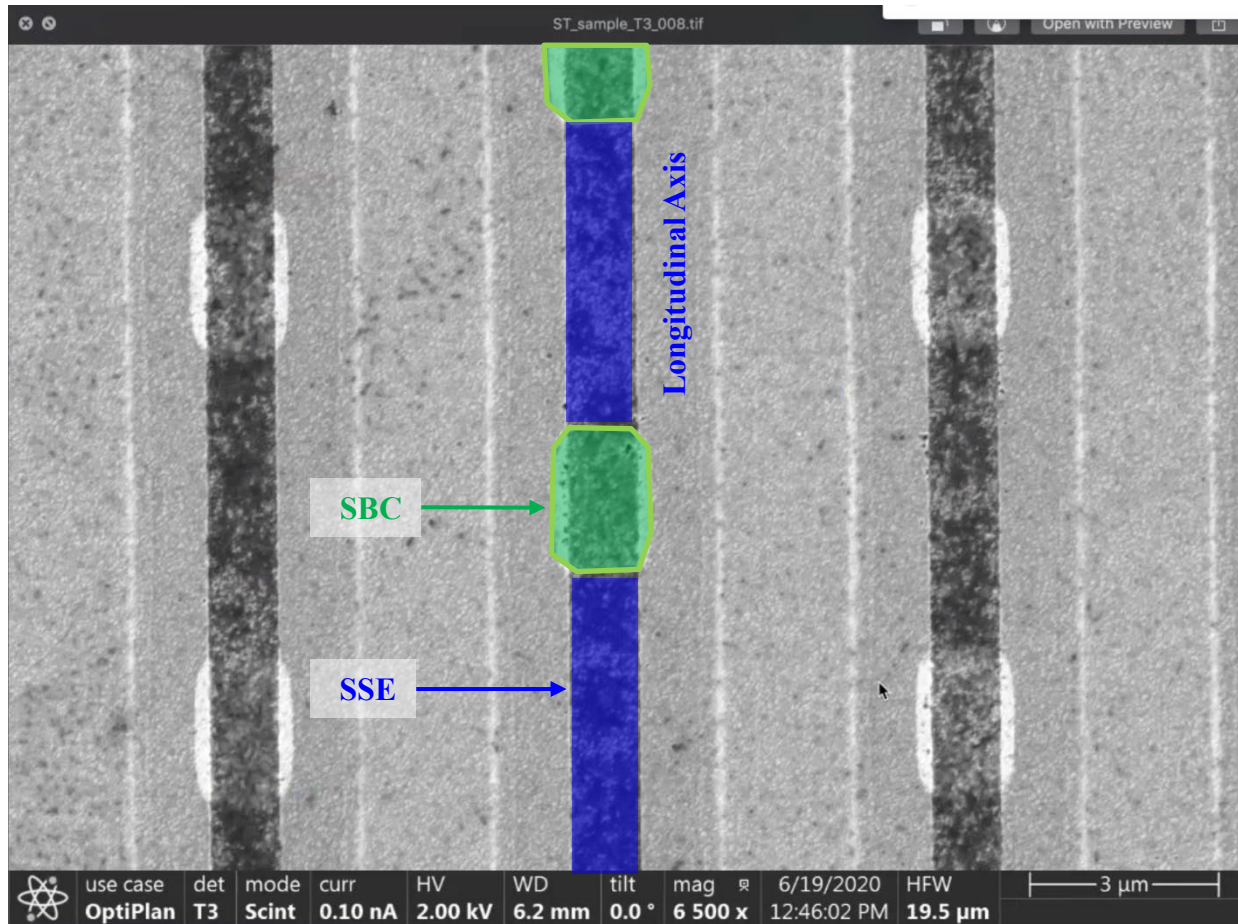
SEM SEPC



Note: SCM view taken at B-B' cross section

Claim 9

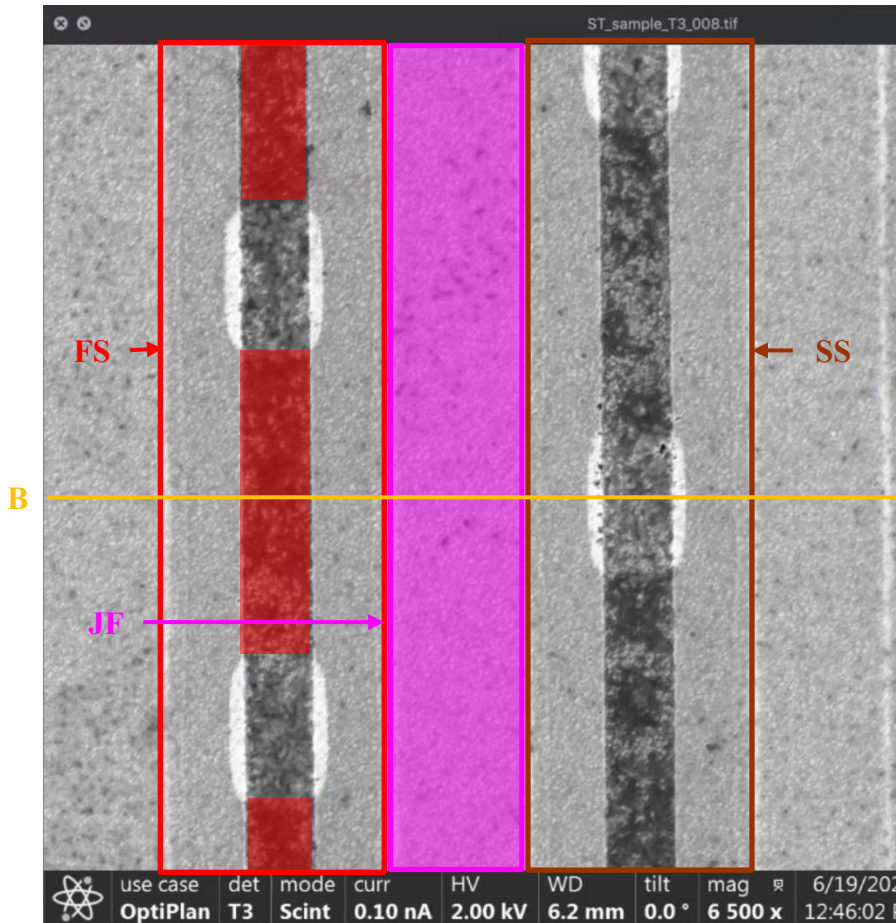
(SBC) each of the plurality of second base contact regions being spaced apart from each other in a (SSE) direction parallel to the longitudinal axis defined by the second source electrode; and



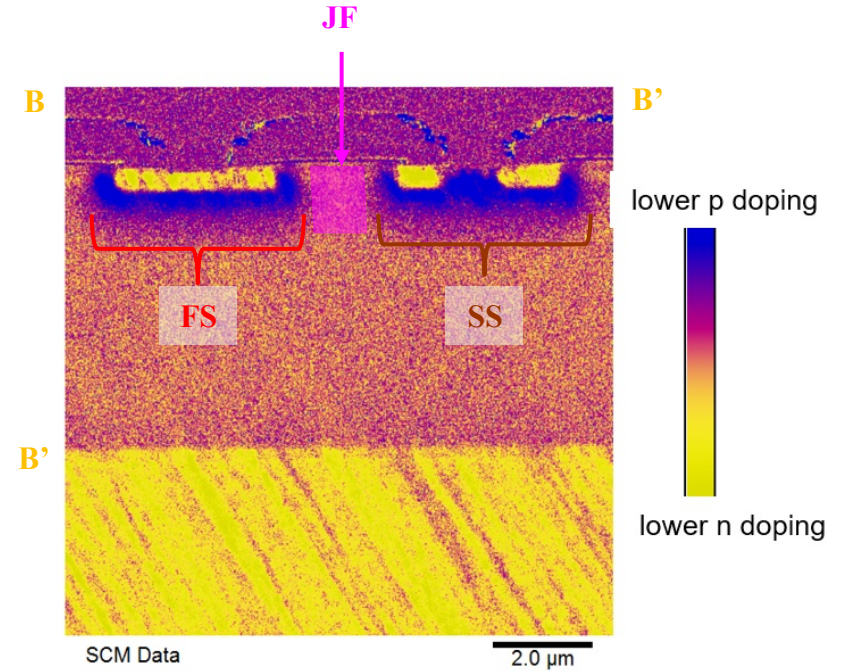
SEM SEPC

Claim 9

a **(JF) JFET region defined between the (FS) first source region and the (SS) second source region,**

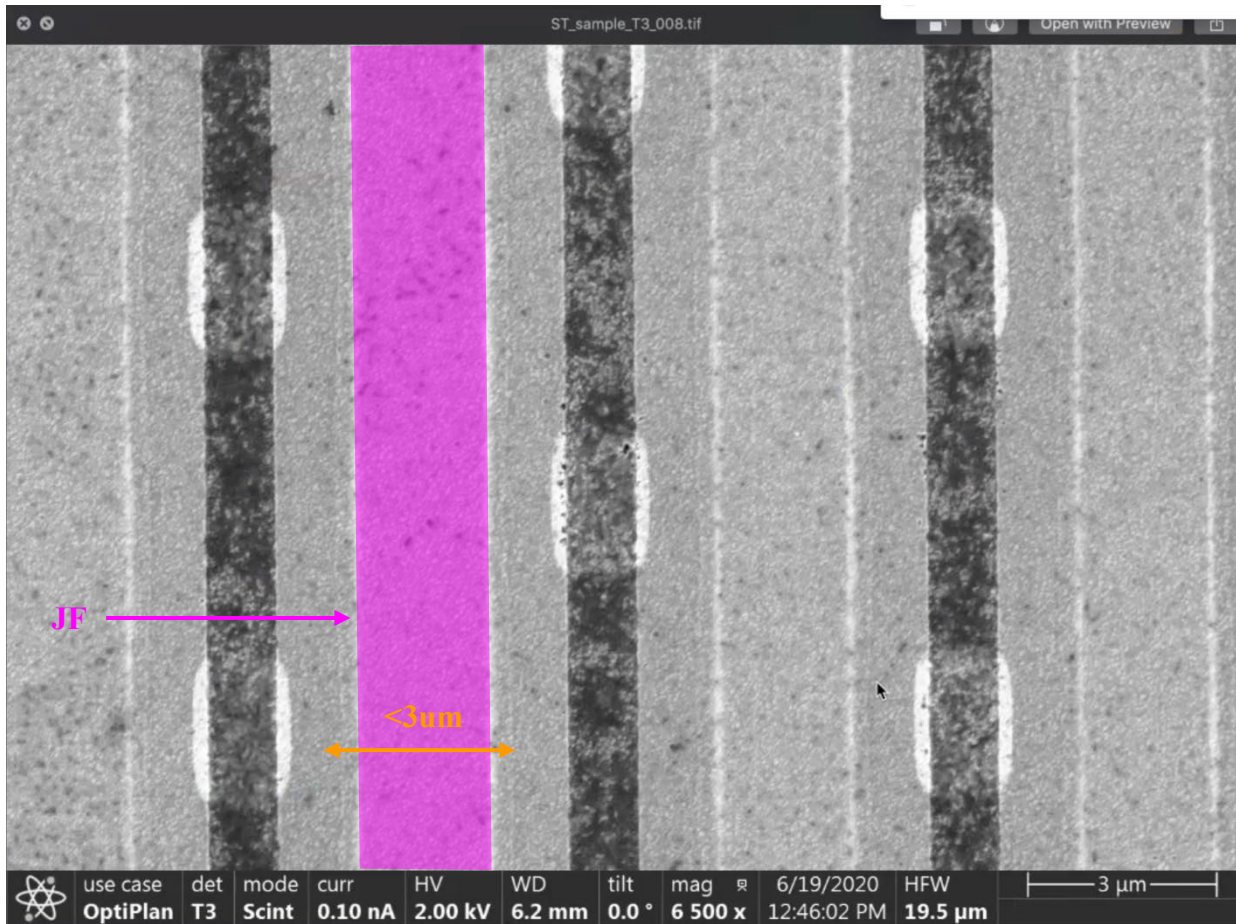


SEM SEPC



Claim 9

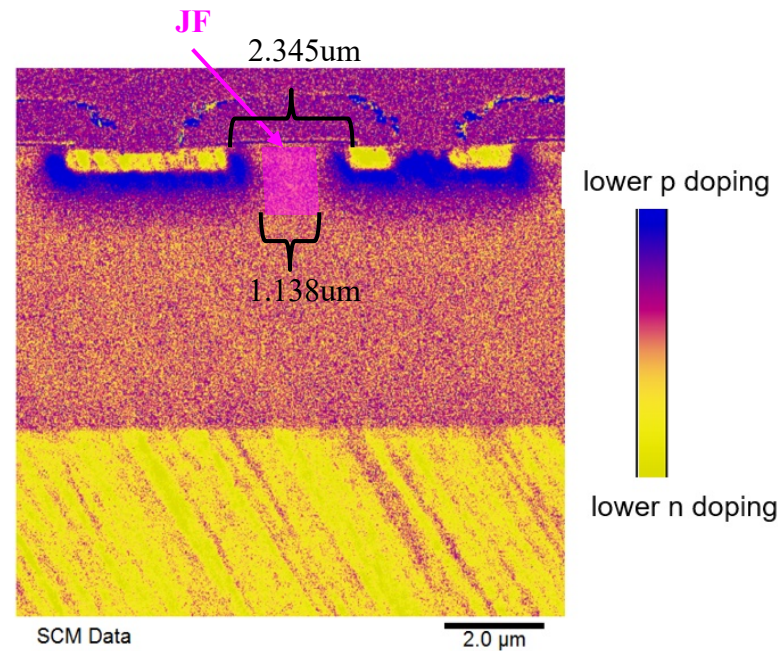
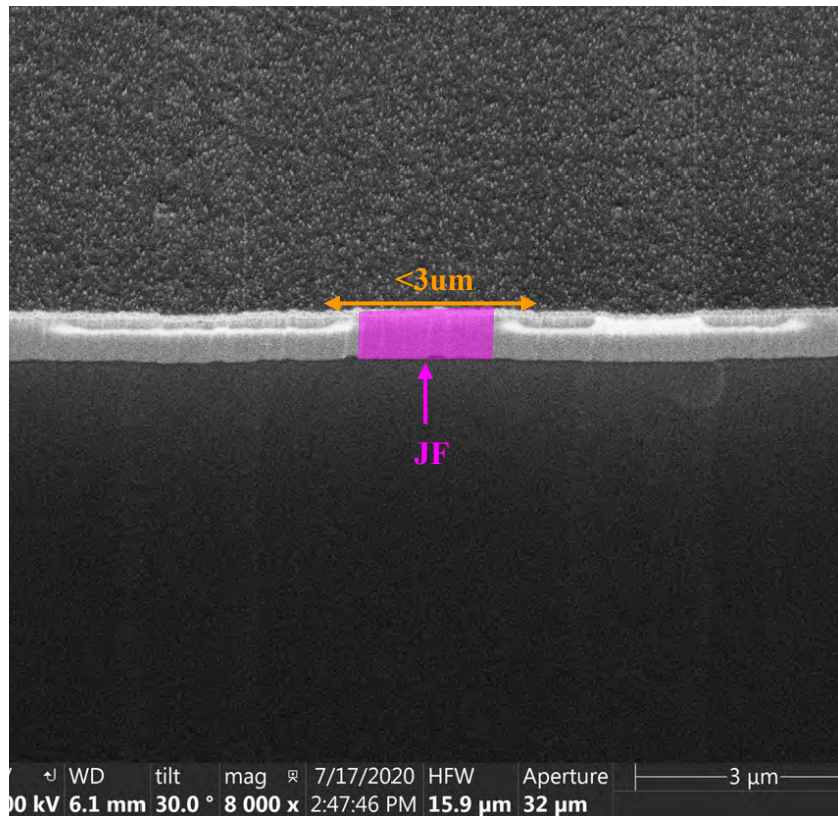
the (JF) JFET region having a width less than about three micrometers.



SEM SEPC

Claim 9

the (JF) JFET region having a width less than about three micrometers.



Note: SEM SEPC taken at B-B' cross section



(10) **Patent No.:** US 7,498,633 B2
(45) **Date of Patent:** Mar. 3, 2009

(56) **References Cited**

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5,545,908	A *	8/1996	Tokura et al.	257:341
6,137,139	A *	10/2000	Zeng et al.	257:342
6,552,391	B2 *	4/2003	Zeng et al.	257:342
6,573,534	B1 *	6/2003	Kumar et al.	257:77
2003-0052329	A1 *	3/2003	Kobayashi et al.	257:135
2003-0205829	A1 *	11/2003	Boden, Jr.	257:921
2003-0227052	A1 *	12/2003	Ono et al.	257:341

6,552,391	B2*	4/2003	Zeng et al.	257/342
6,573,534	B1*	6/2003	Kumar et al.	257/77
2003/0052329	A1*	3/2003	Kobayashi et al.	257/135
2003/0205829	A1*	11/2003	Boden, Jr.	257/921
2003-0227052	A1*	12/2003	Ono et al.	257/341

2003/0205829	A1*	11/2003	Boden, Jr.	257/921
2003/0227052	A1*	12/2003	Ono et al.	257/341

* cited by examiner

Primary Examiner—Zandra Smith
Assistant Examiner—Paul E Patton
(74) Attorney, Agent, or Firm—Barnes & Thornburg LLP

(57) **ABSTRACT**

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(57) **ABSTRACT**



Exemplary Claim: 9

Claim 9

A **double-implanted metal-oxide semiconductor field-effect transistor** comprising:

a **(SUB) silicon-carbide substrate**;

a **(DL) drift semiconductor layer** formed on a **(FS) front side** of the **(SUB) semiconductor substrate**;

a **(FS) first source region**;

a **(FSE) first source electrode** formed over the **(FS) first source region**, the **(FSE) first source electrode defining a longitudinal axis**;

a **(FBC) plurality of first base contact regions** defined in the **(FS) first source region**, **(FBC) each of the plurality of first base contact regions being spaced apart from each other** in a **(FSE) direction parallel to the longitudinal axis defined by the first source electrode**;

a **(SS) second source region**;


a **(SSE) second source electrode** formed over the **(SS) second source region**, the **(SSE) second source electrode defining a longitudinal axis**;

a **(SBC) plurality of second base contact regions** defined in the **(SS) second source region**, **(SBC) each of the plurality of second base contact regions being spaced apart from each other** in a **(SSE) direction parallel to the longitudinal axis defined by the second source electrode**; and

a **(JF) JFET region defined between** the **(FS) first source region** and the **(SS) second source region**, the **(JF) JFET region having a width less than about three micrometers**.

Claim 9

A **double-implanted metal-oxide semiconductor field-effect transistor** comprising:

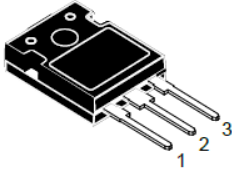


life.augmented

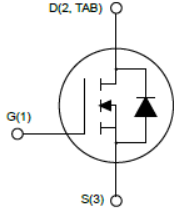
SCTW70N120G2V

Datasheet

Silicon carbide Power MOSFET 1200 V, 91 A, 21 mΩ (typ., $T_J = 25\text{ }^{\circ}\text{C}$)
in an HiP247 package



HiP247



AM01475v1_no2en

Features

Order code	V_{DS}	$R_{DS(on)}$ typ.	I_D
SCTW70N120G2V	1200 V	21 mΩ	91 A

- Very high operating junction temperature capability ($T_J = 200\text{ }^{\circ}\text{C}$)
- Very fast and robust intrinsic body diode
- Extremely low gate charge and input capacitances

Applications

- Charger
- Power supply for renewable energy systems
- High frequency DC-DC converters

Description

This silicon carbide Power MOSFET is produced exploiting the advanced, innovative properties of wide bandgap materials. This results in unsurpassed on-resistance per unit area and very good switching performance almost independent of temperature. The outstanding thermal properties of the SiC material allow designers to use an industry-standard outline with significantly improved thermal capability. These features render the device perfectly suitable for high-efficiency and high power density applications.

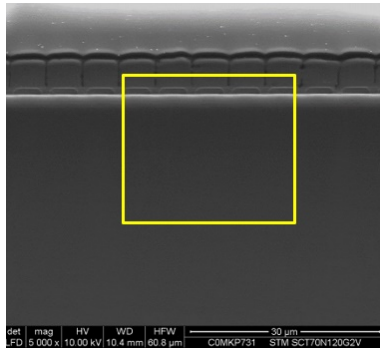
Claim 9

A **double-implanted metal-oxide semiconductor field-effect transistor** comprising:



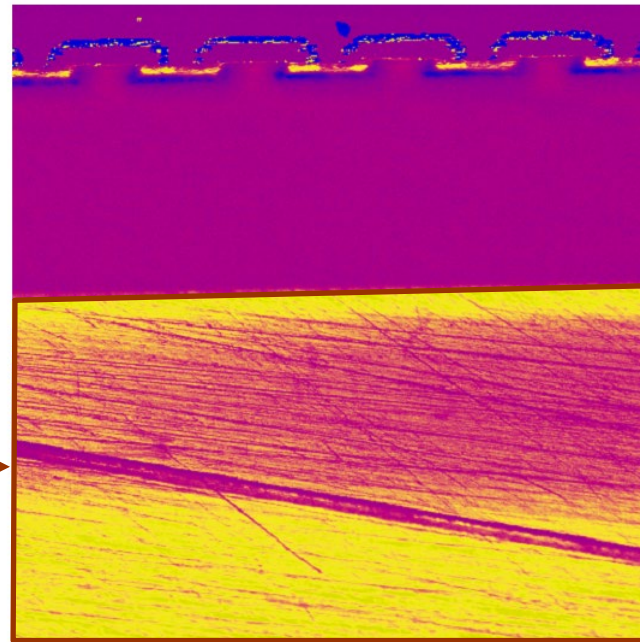
Claim 9

a (SUB) silicon-carbide substrate;



SEM

SUB →



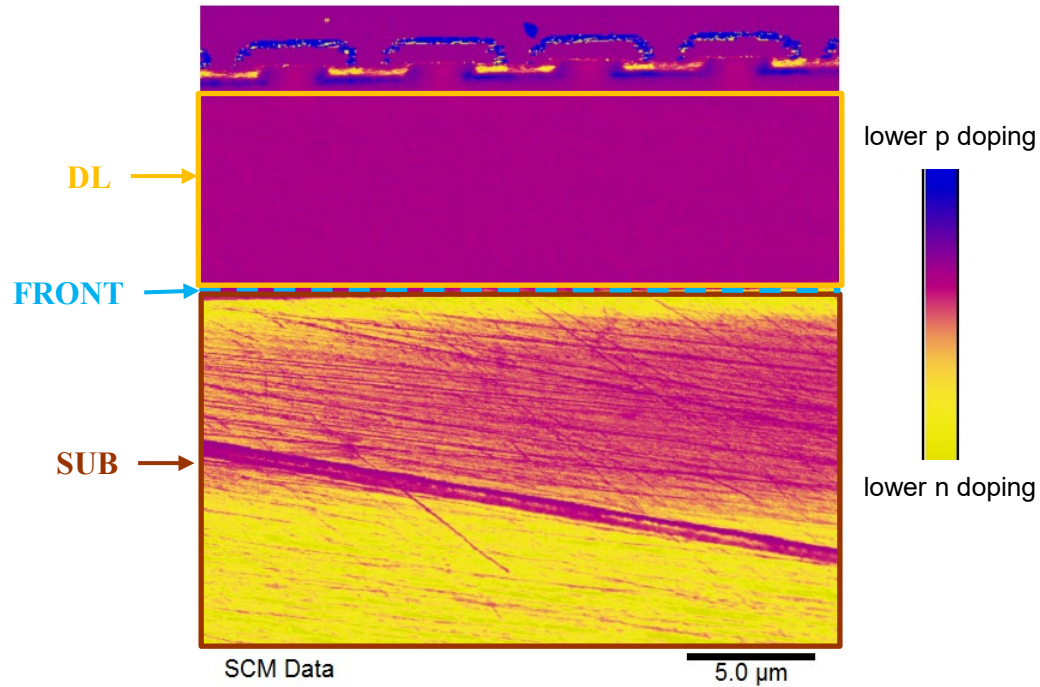
SCM Data

5.0 µm

Note: Scanning Capacitance Microscopy (SCM) taken of the framed area in the Scanning Electron Microscopy (SEM) image

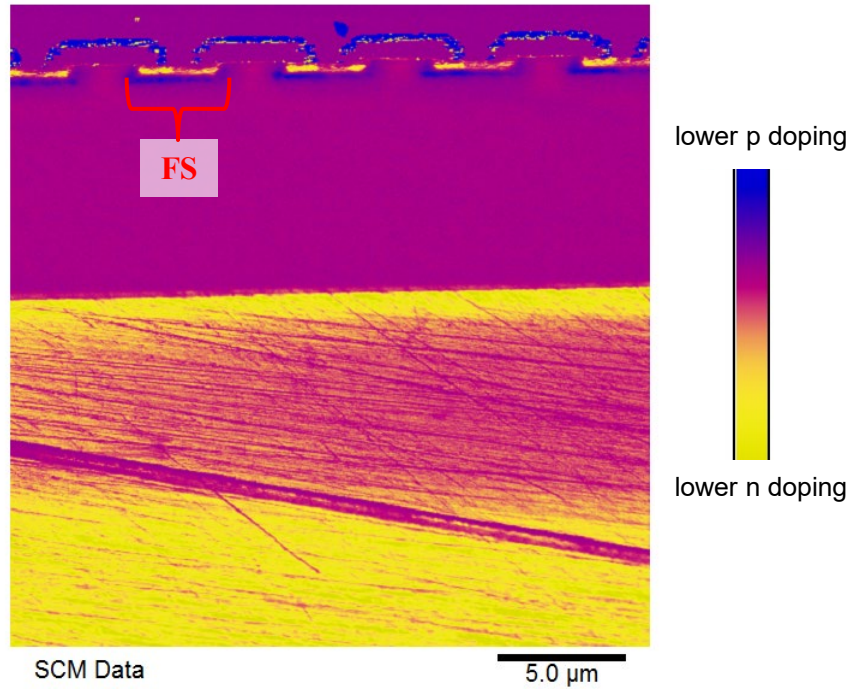
Claim 9

a **(DL)** drift semiconductor layer formed on a **(FRONT)** front side of the **(SUB)** semiconductor substrate;



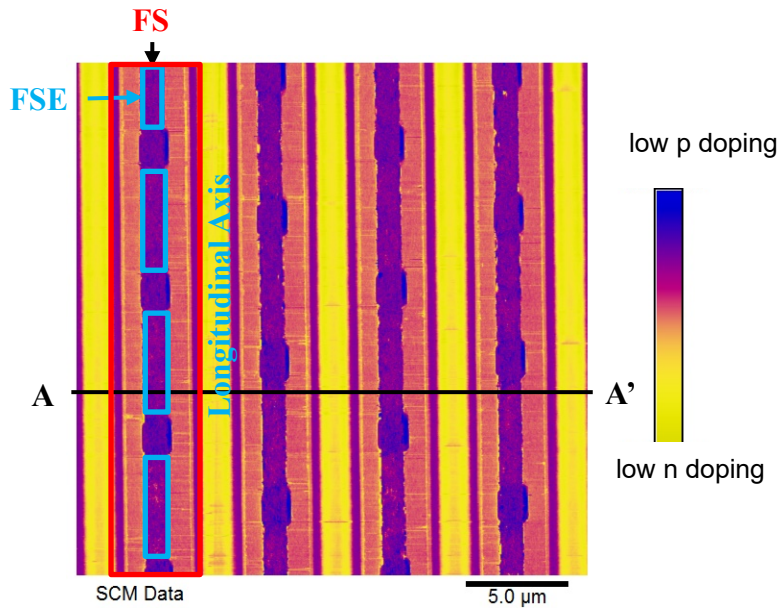
Claim 9

a **(FS) first source region;**

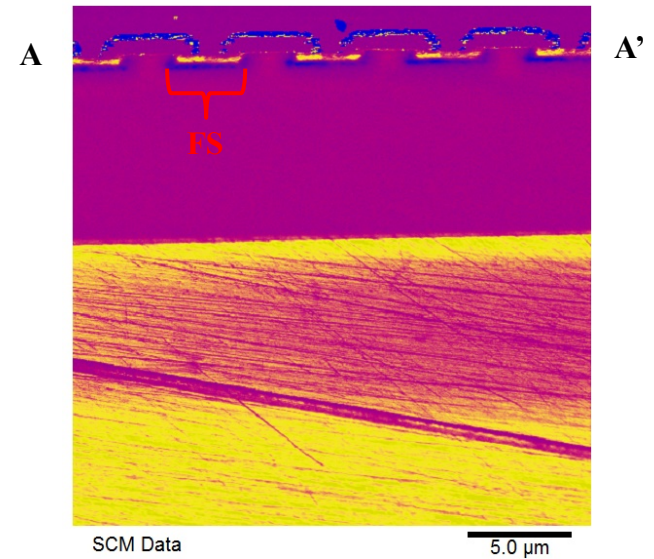


Claim 9

a (FSE) first source electrode formed over the (FS) first source region, the (FSE) first source electrode defining a longitudinal axis;



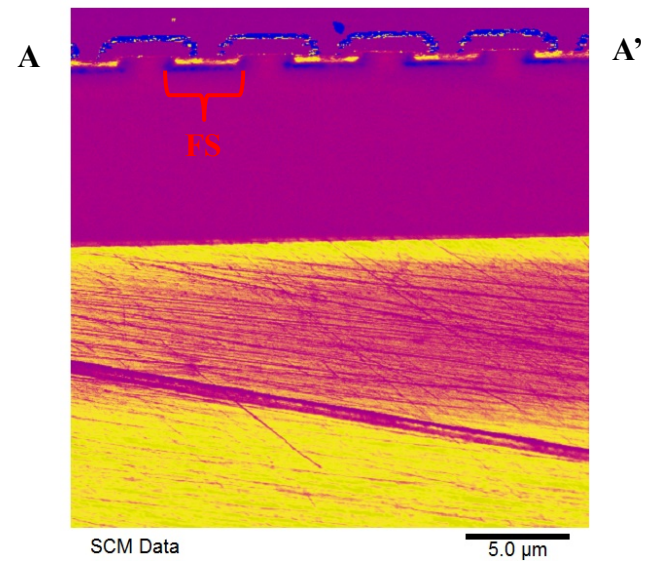
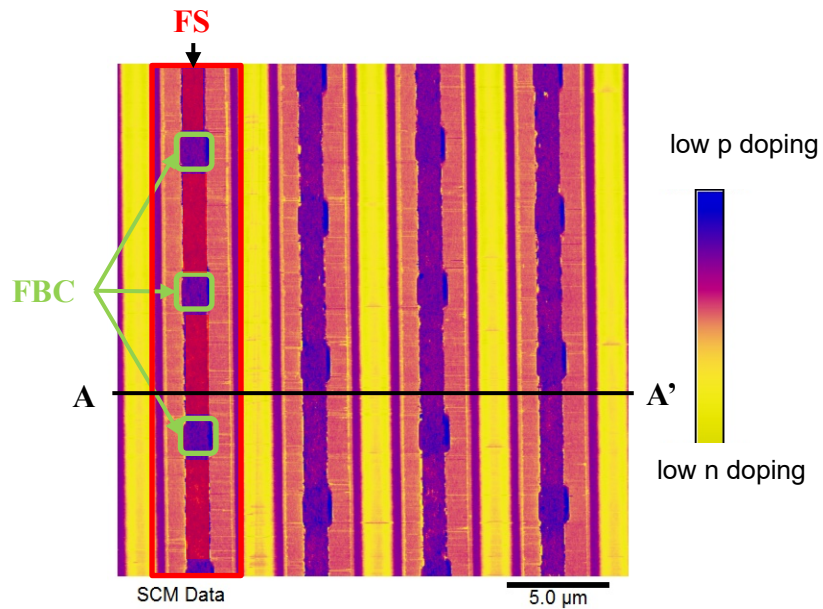
Note: Top view using SCM, after polishing down to the silicon carbide.



Note: SCM view taken at the A-A' cross-section.

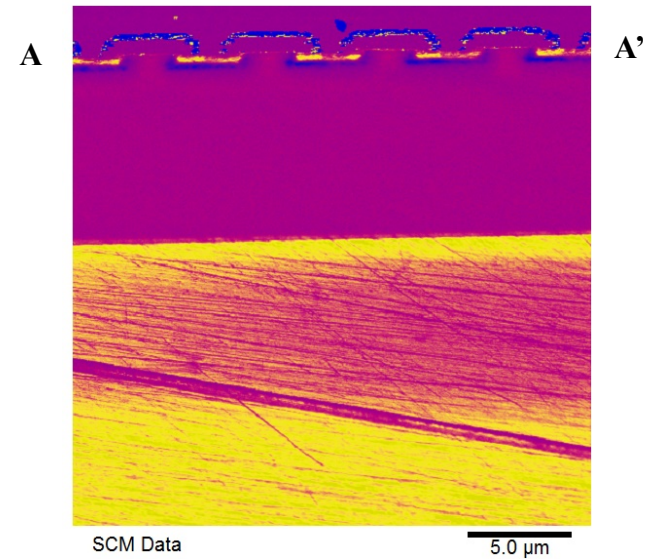
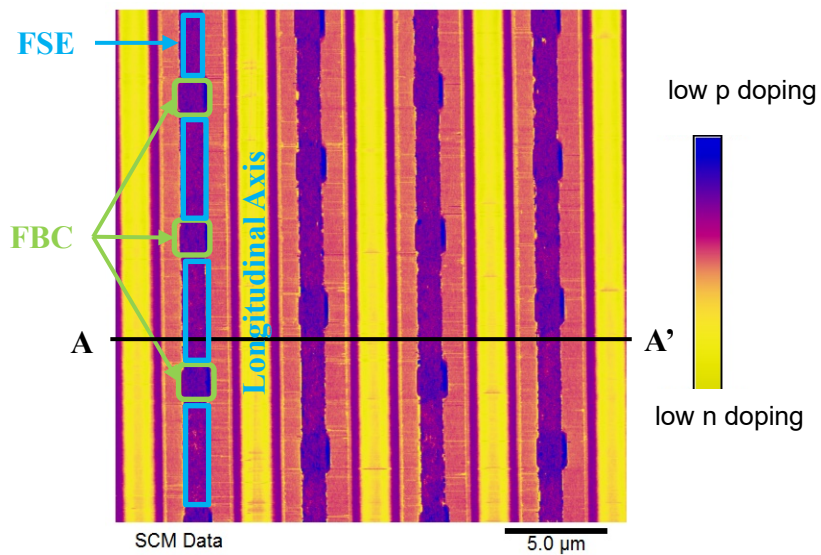
Claim 9

a (FBC) plurality of first base contact regions defined in the (FS) first source region,



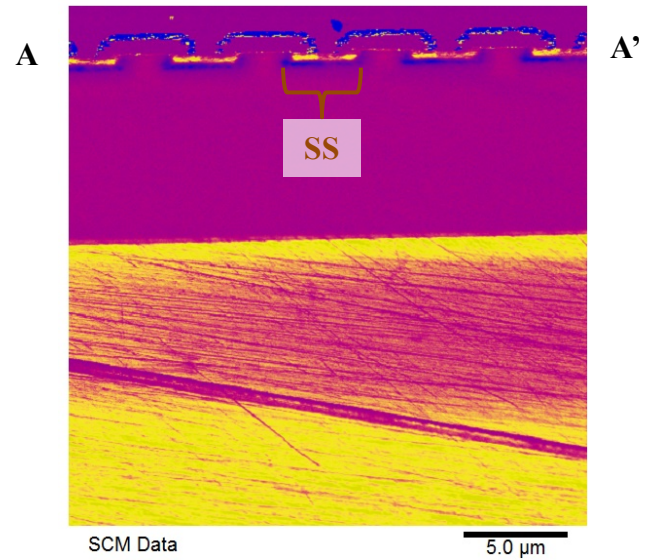
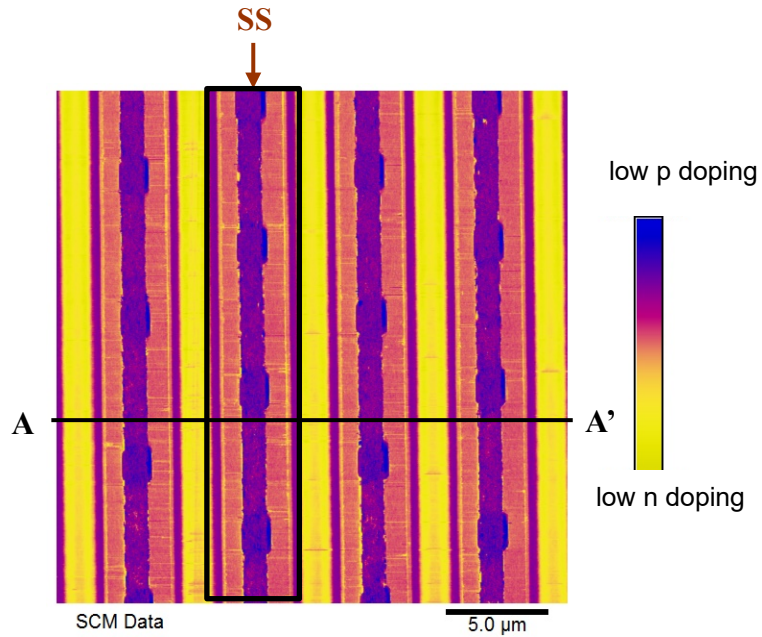
Claim 9

(FBC) each of the plurality of first base contact regions being spaced apart from each other in a (FSE) direction parallel to the longitudinal axis defined by the first source electrode;



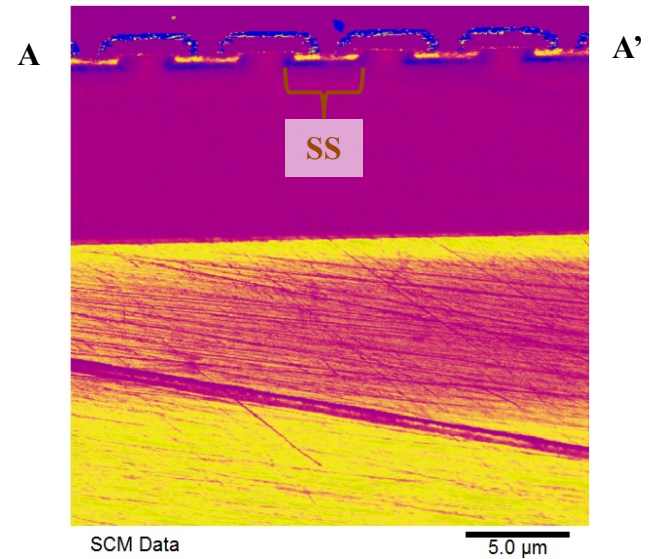
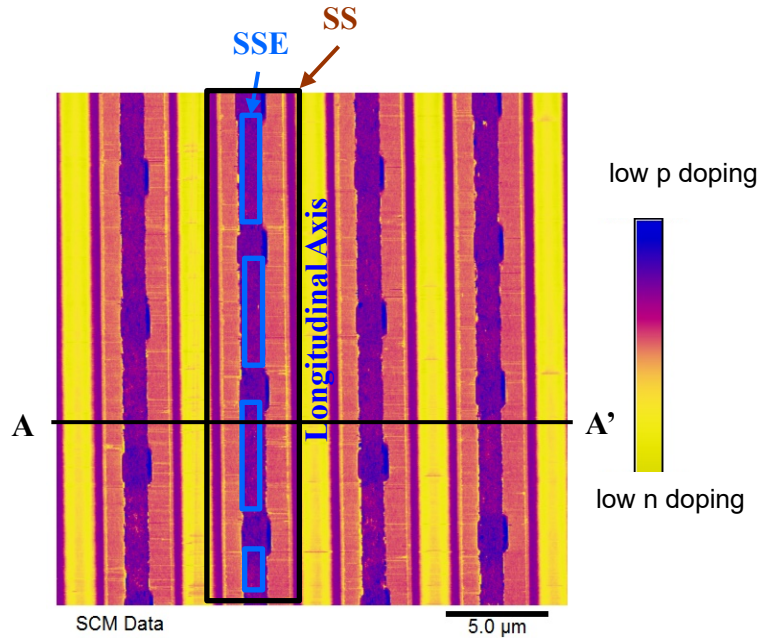
Claim 9

a (SS) second source region;



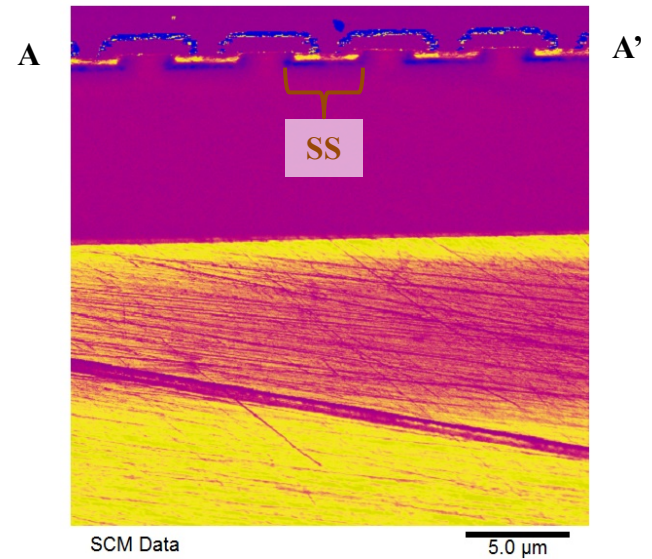
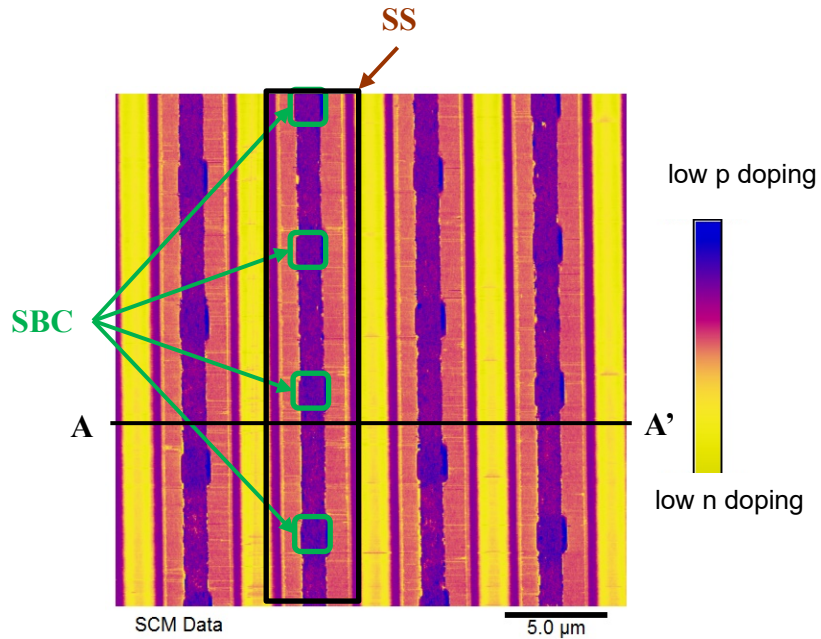
Claim 9

a (SSE) second source electrode formed over the (SS) second source region, the (SSE) second source electrode defining a longitudinal axis;



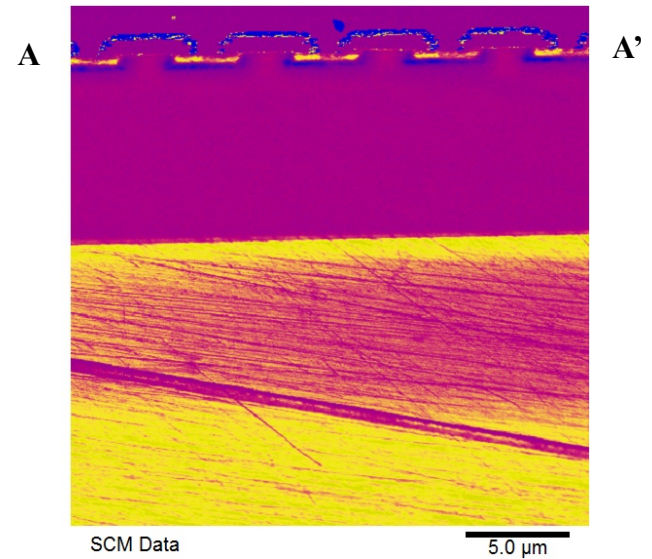
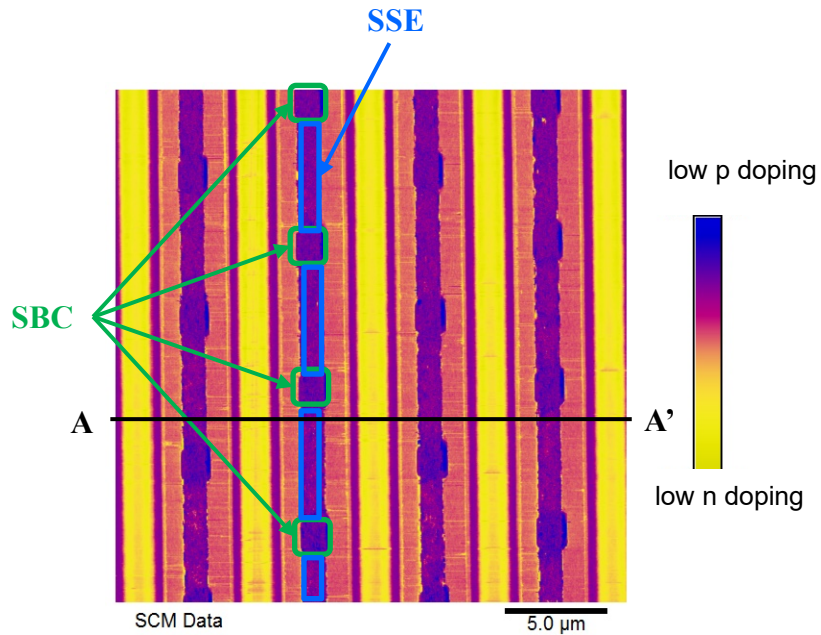
Claim 9

a (SBC) plurality of second base contact regions defined in the (SS) second source region,



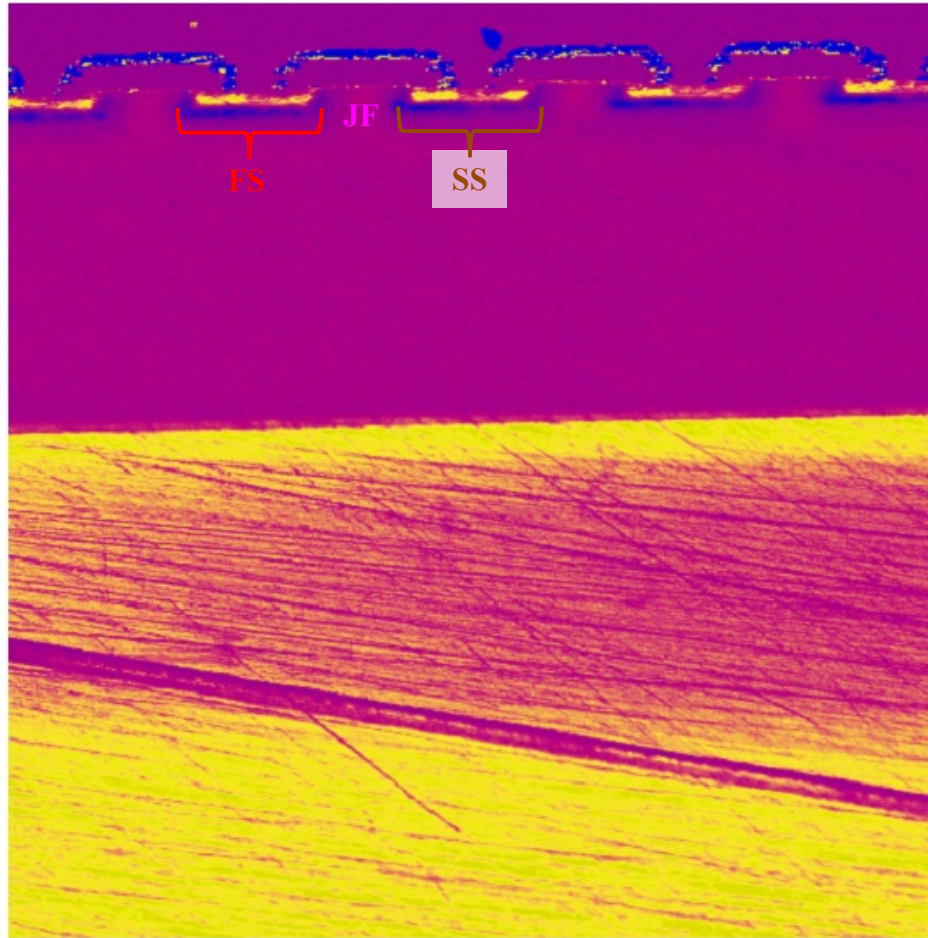
Claim 9

(SBC) each of the plurality of second base contact regions being spaced apart from each other in a (SSE) direction parallel to the longitudinal axis defined by the second source electrode; and



Claim 9

a **(JF) JFET region defined between** the **(FS) first source region** and the **(SS) second source region**,

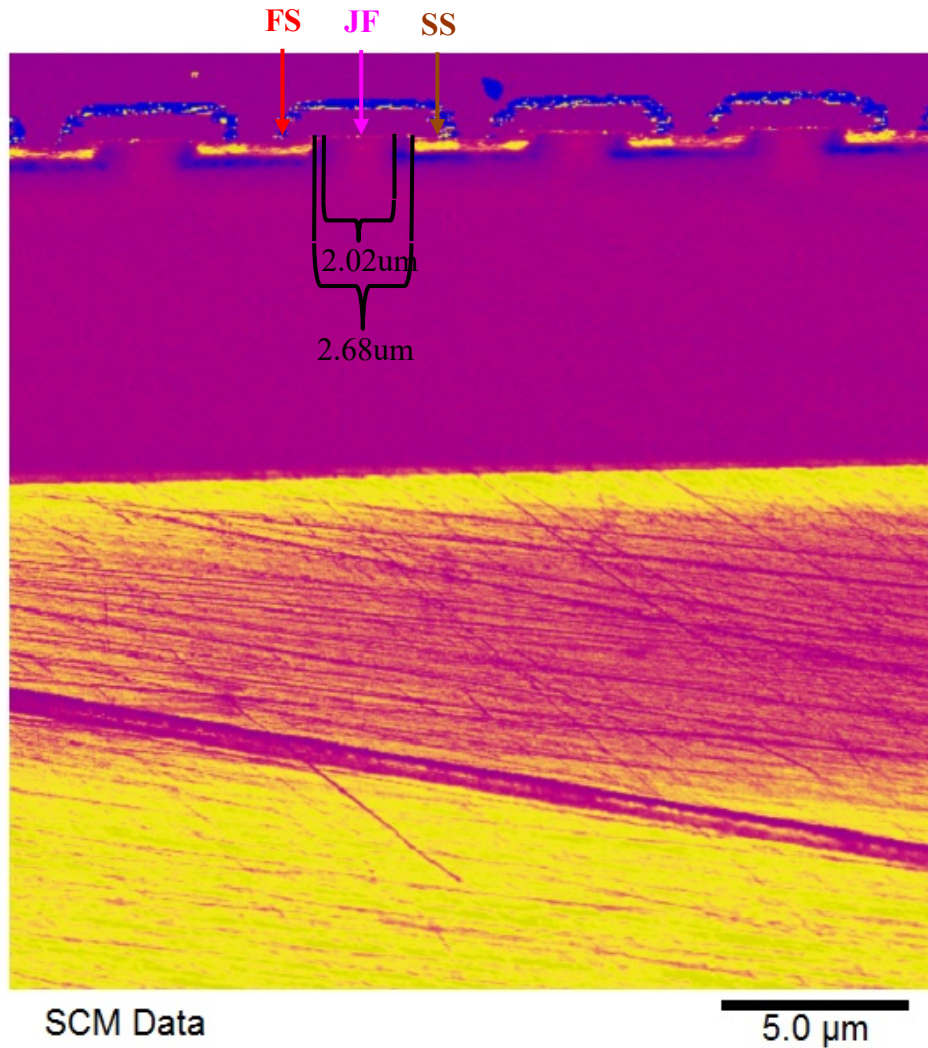



SCM Data

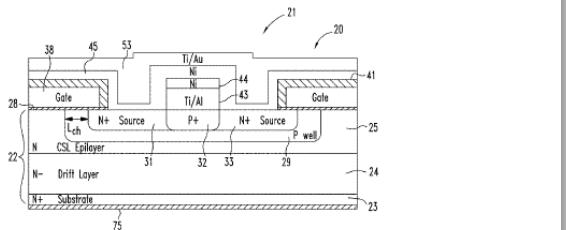
5.0 μm

Claim 9

the (JF) JFET region having a width less than about three micrometers.



 US008035112B1		
(12) United States Patent Cooper et al.	(10) Patent No.: US 8,035,112 B1	(45) Date of Patent: Oct. 11, 2011
(54) SIC POWER DMOSFET WITH SELF-ALIGNED SOURCE CONTACT		
(75) Inventors: James A. Cooper, West Lafayette, IN (US); Asmita Saha, Hillsboro, OR (US)		
(73) Assignee: Purdue Research Foundation, West Lafayette, IN (US)		
(*) Notice: Subject to any disclaimer, the term of this patent is extended or adjusted under 35 U.S.C. 154(b) by 91 days.		
(21) Appl. No.: 12/429,176		
(22) Filed: Apr. 23, 2009		
Related U.S. Application Data		
(60) Provisional application No. 61/047,274, filed on Apr. 23, 2008.		
(51) Int. Cl. H01L 21/0312 (2006.01)		
(52) U.S. Cl. 257/77; 257/76; 438/142		
(58) Field of Classification Search 257/77; 257/76; 438/105; 142		
See application file for complete search history.		
(56) References Cited		
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4,070,690 A 1/1978 Wickstrom 4,893,160 A 1/1990 Blanchard 5,506,421 A 4/1996 Palmour 5,637,898 A 6/1997 Baliga 5,780,324 A 7/1998 Tokura et al. 5,786,251 A 7/1998 Harris et al. 5,801,417 A 9/1998 Tsang et al. 5,814,859 A 9/1998 Chetani et al. 6,054,752 A 4/2000 Han et al. 6,150,671 A 11/2000 Harris et al. 6,180,958 B1 1/2001 Cooper 6,238,980 B1 5/2001 Ueno		
6,297,100 B1 10/2001 Kumar et al. 6,316,906 B1 11/2001 Mo 6,344,663 B1 2/2002 Slater et al. 6,362,495 B1 3/2002 Schoen et al. 6,465,807 B1 10/2002 Ueno 6,573,534 B1 * 6/2003 Kumar et al. 6,737,677 B2 5/2004 Shimoda et al. 6,815,293 B2 * 11/2004 Dunney et al. 6,894,319 B2 5/2005 Kobayashi et al. 7,074,643 B2 7/2006 Ryu 7,498,633 B2 3/2009 Cooper et al. 7,521,731 B2 * 4/2009 Shimoda et al. 7,622,741 B2 * 11/2009 Munn 2003/0073,270 A1 * 4/2003 Hosoda et al. 2004/0145,011 A1 7/2004 Imai et al. 2006/0065,925 A1 3/2006 Yoshida 2007/0209,968 A1 11/2007 Saxler et al.		
OTHER PUBLICATIONS		
U.S. Appl. No. 10/821,613, filed Apr. 9, 2004, Cooper et al. U.S. Appl. No. 12/429,153, filed Apr. 23, 2009, Cooper et al. B. Jayar Baliga, "Power Semiconductor Devices," PWS Publishing Co., 1996, Ch. 7, "Power MOSFET," pp. 335-421.		
(74) Attorney, Agent, or Firm — Phuc Dung Randall Frisk		
(57) ABSTRACT		
An intermediate product in the fabrication of a MOSFET, including a silicon carbide wafer having a substrate and a drift layer on said substrate, said drift layer having a plurality of source regions formed adjacent an upper surface thereof; a first oxide layer on said upper surface of said drift layer; a plurality of polysilicon gates above said first oxide layer, said plurality of polysilicon gates including a first gate adjacent a first of said source regions; an oxide layer over said first source region of greater thickness than said first oxide layer; and, an oxide layer over said first gate of substantially greater thickness than said oxide layer over said first source region.		
16 Claims, 5 Drawing Sheets		



Title: SIC POWER DMOSFET WITH SELF-ALIGNED SOURCE CONTACT

Priority Date: April 23, 2008

Filed Date: April 23, 2009

Issued Date: October 11, 2011

Expiration Date: July 23, 2029

Inventors: James A. Cooper; Asmita Saha

Exemplary Claim: 1

Claim 1

A **silicon carbide power MOSFET**, comprising:

- a **(SUB) silicon carbide wafer having a substrate** and a **(DFT) drift layer** on said **substrate**, said **(DFT) drift layer** having a **(SR) plurality of source regions formed adjacent** an **(US) upper surface** thereof;
- a **(GAT) plurality of polysilicon gates above** said **(DFT) drift layer**, said **(GAT) plurality of polysilicon gates** including a **(GAT1) first gate** adjacent a **(SR1) first of said source regions**,
- said **(GAT1) first gate** having a **(TOP) top surface**, a **(BOT) lower surface** and a **(SW) sidewall**, said **(SW) sidewall overlying** said **(SR1) first source region**;
- a **(SOX) first oxide layer between** said **(BOT) first gate lower surface** and said **(US) upper surface** of said **(DFT) drift layer**;
- a **(ILD) second, thicker oxide layer** over said **(TOP) top surface** and **(SW) sidewall** of said **(GAT1) first gate**;
- and
- a **(ML) conformal layer of metal** extending laterally across said **(GAT1) first gate (TOP) top surface** and **(SW) sidewall** and said **adjacent (SR1) first source region**.

Claim 1

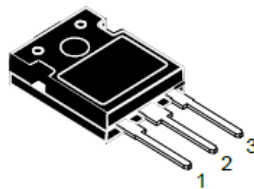
A **silicon carbide power MOSFET**, comprising:



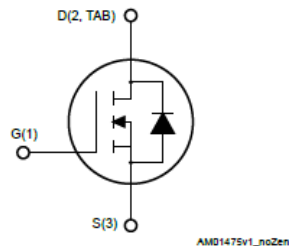
SCTW90N65G2V

Datasheet

Silicon carbide Power MOSFET 650 V, 119 A, 18 mΩ (typ., $T_J = 25\text{ }^{\circ}\text{C}$)
in an HiP247 package



HiP247



AIM01475v1_no2en

Features

Order code	V_{DS}	$R_{DS(on)}$ max.	I_D
SCTW90N65G2V	650 V	24 mΩ	119 A

- Very high operating junction temperature capability ($T_J = 200\text{ }^{\circ}\text{C}$)
- Very fast and robust intrinsic body diode
- Extremely low gate charge and input capacitances

Applications

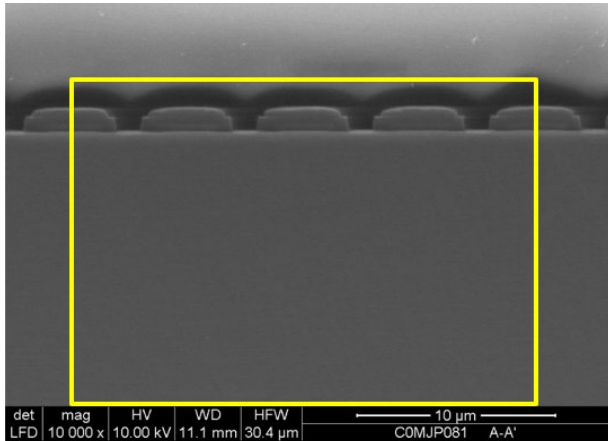
- Switching applications
- Power supply for renewable energy systems
- High frequency DC-DC converters

Description

This silicon carbide Power MOSFET device has been developed using ST's advanced and innovative 2nd generation SiC MOSFET technology. The device features remarkably low on-resistance per unit area and very good switching performance. The variation of switching loss is almost independent of junction temperature.

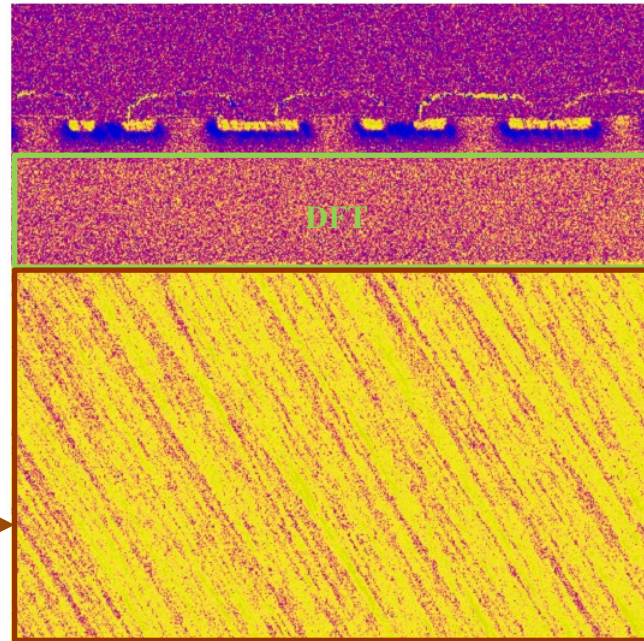
Claim 1

a **(SUB)** silicon carbide wafer having a **substrate** and a **(DFT)** drift layer on said **substrate**,



SEM

SUB →



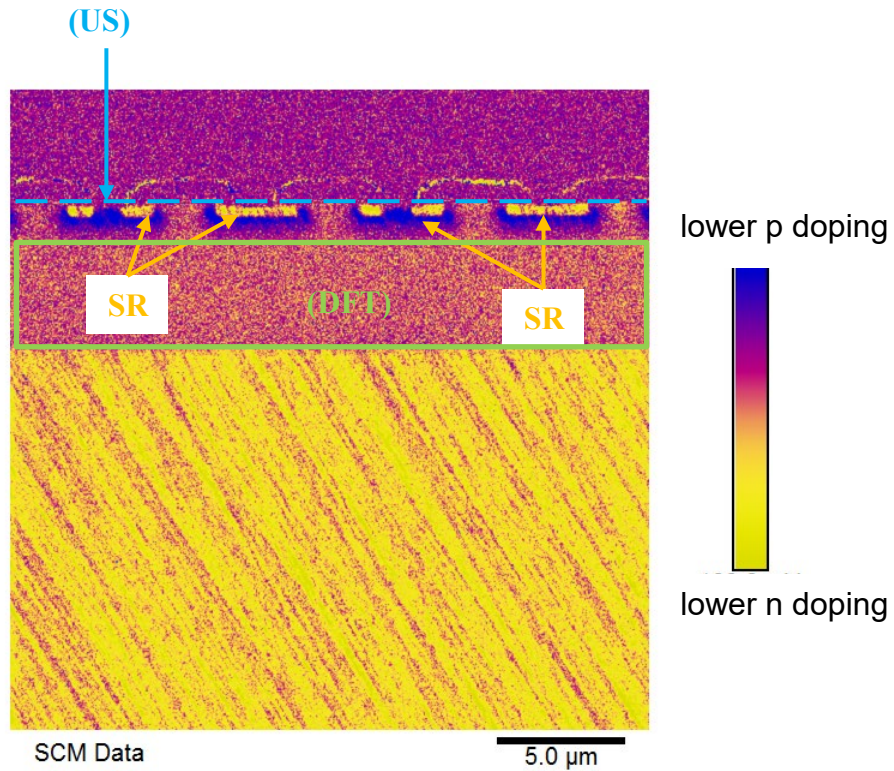
SCM Data

5.0 μm

Note: Scanning Capacitance Microscopy (SCM) of the framed area in the Scanning Electron Microscopy (SEM) image.

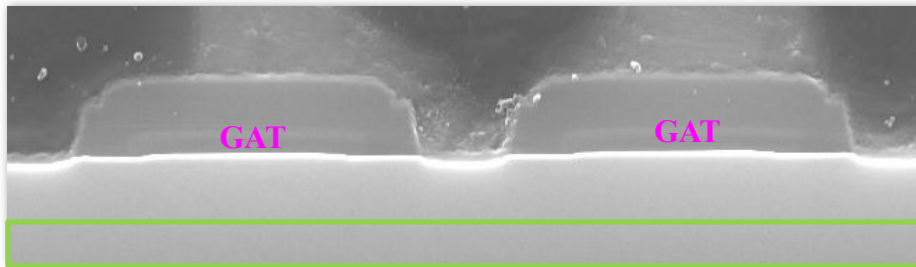
Claim 1

said (DFT) drift layer having a (SR) plurality of source regions formed adjacent an (US) upper surface thereof;



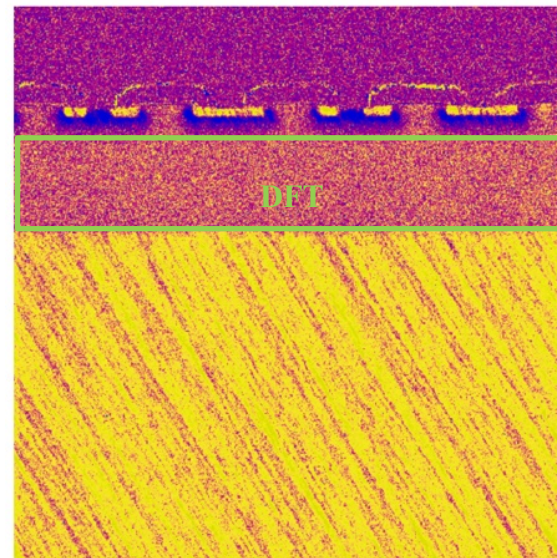
Claim 1

a (GAT) plurality of polysilicon gates above said (DFT) drift layer,



DFT

SEM



SCM Data

5.0 μm

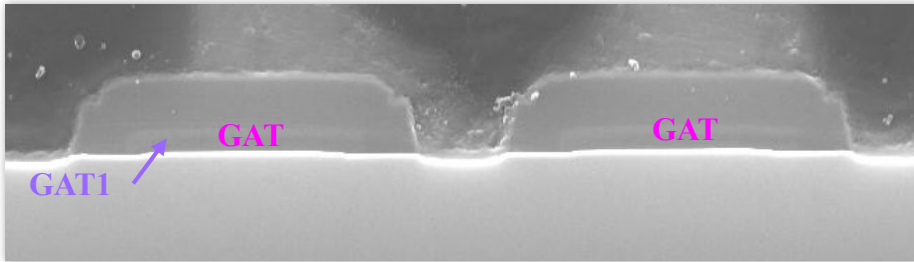
lower p doping



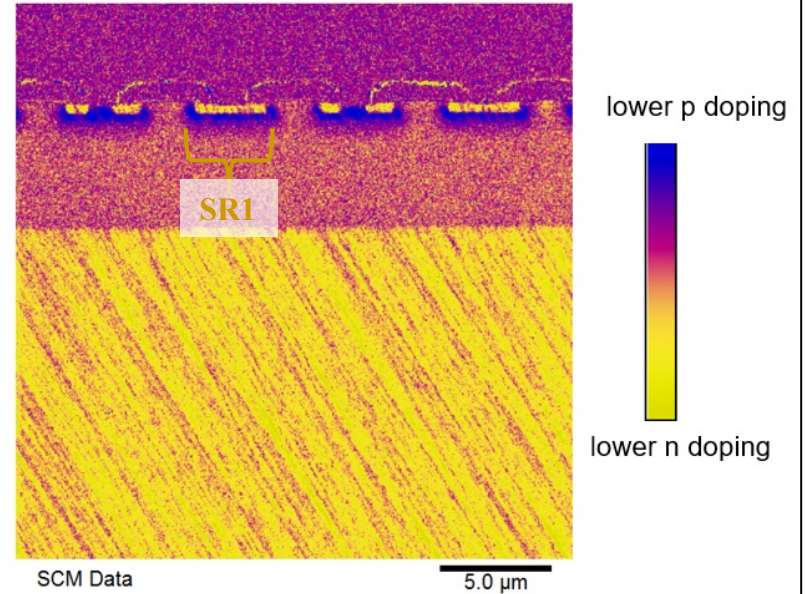
lower n doping

Claim 1

said **(GAT) plurality of polysilicon gates** including a **(GAT1) first gate** adjacent a **(SR1) first of said source regions**,

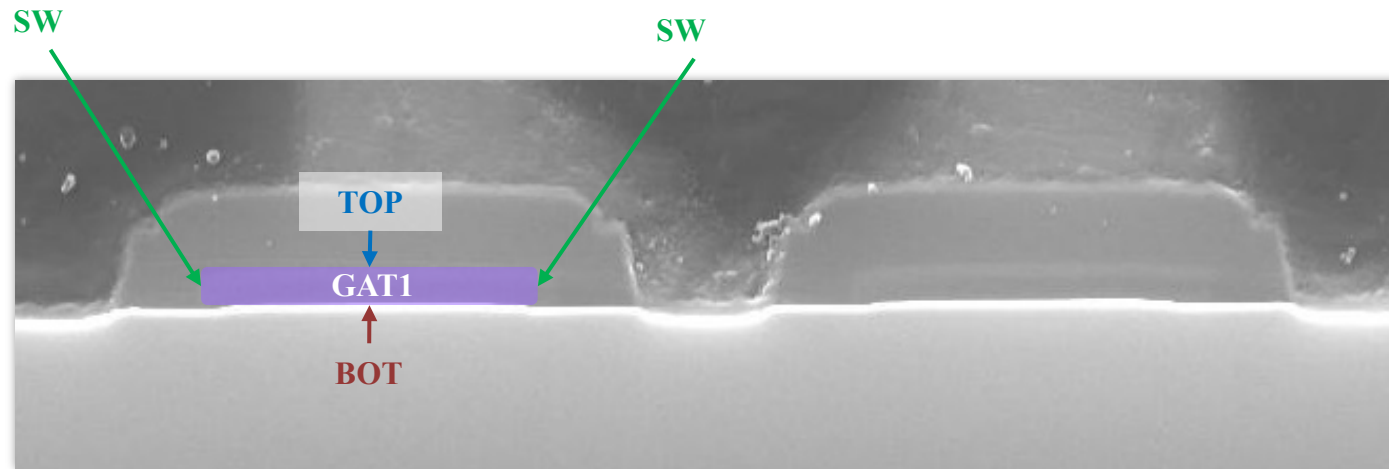


SEM



Claim 1

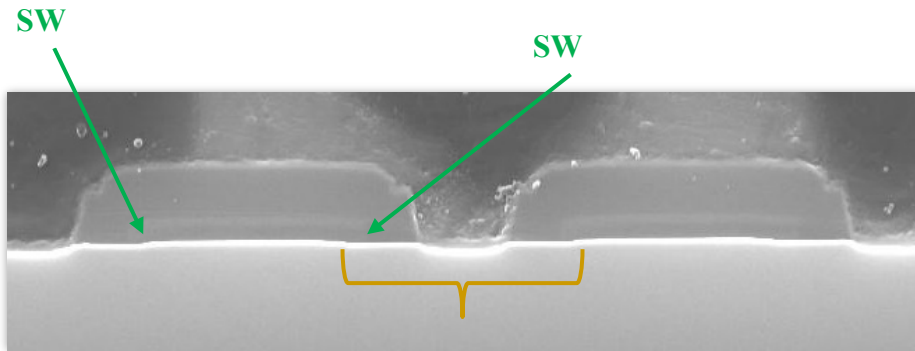
said (GAT1) first gate having a (TOP) top surface, a (BOT) lower surface and a (SW) sidewall,



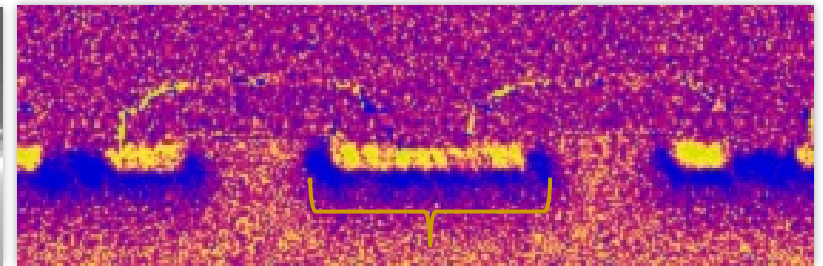
SEM

Claim 1

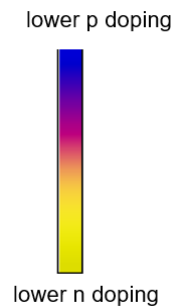
said (SW) sidewall overlying said (SR1) first source region;



SR1
SEM

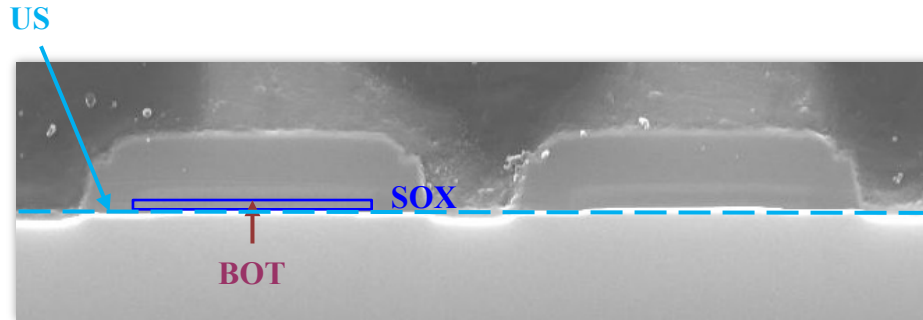


SR1
SCM

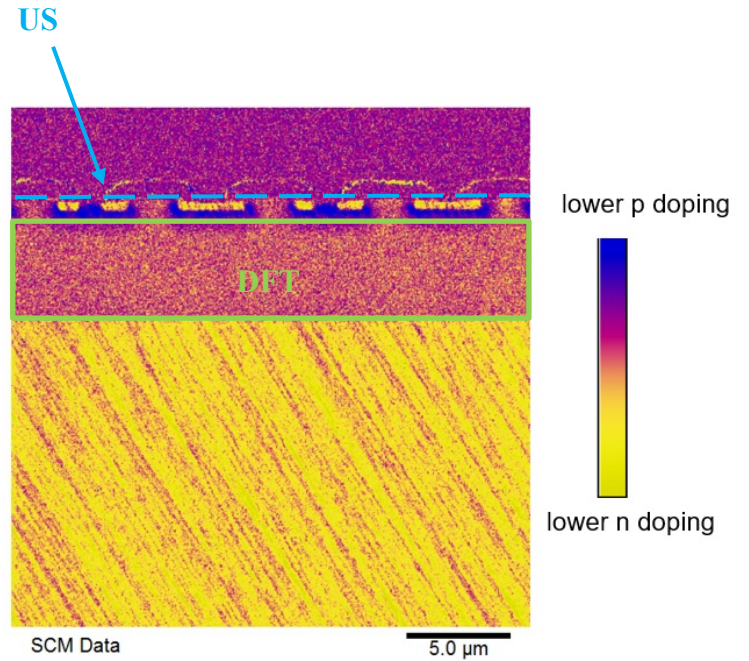


Claim 1

a (SOX) first oxide layer between said (BOT) first gate lower surface and said (US) upper surface of said (DFT) drift layer;

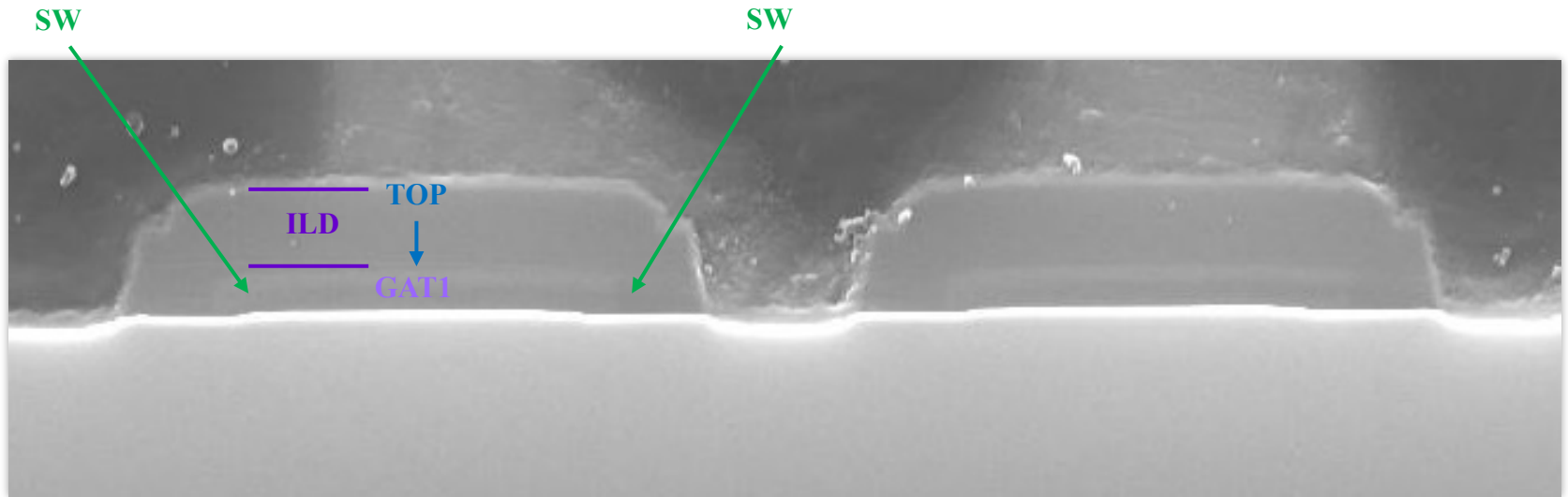


SEM



Claim 1

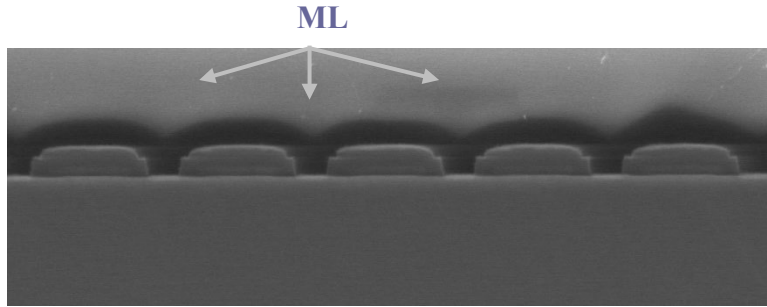
a (ILD) second, thicker oxide layer over said (TOP) top surface and (SW) sidewall of said (GAT1) first gate; and



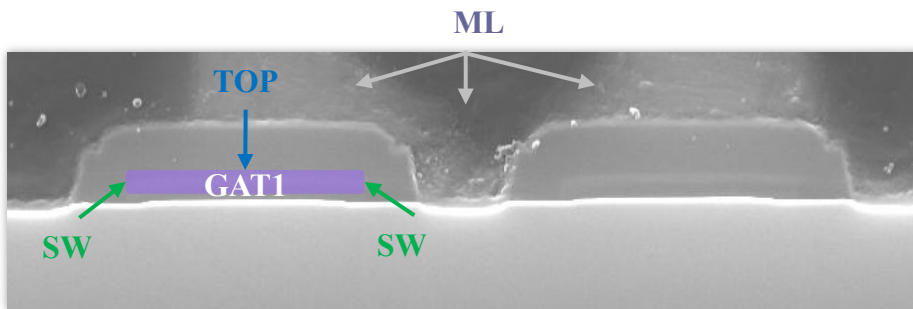
SEM

Claim 1

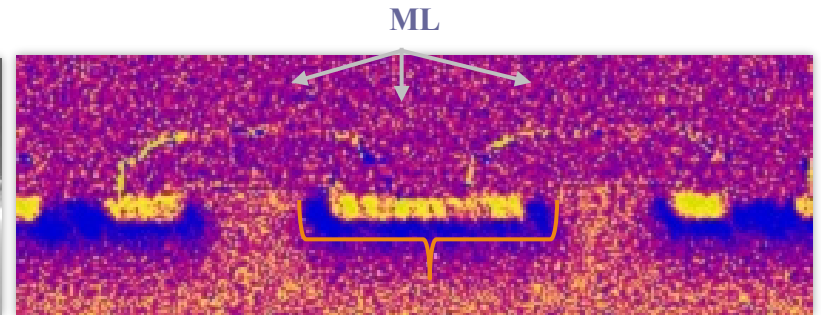
a (ML) conformal layer of metal extending laterally across said (GAT1) first gate (TOP) top surface and (SW) sidewall and said adjacent (SR1) first source region.



SEM



SEM



SR1

SCM



US008035112B1

(12) **United States Patent**
Cooper et al.

(10) **Patent No.:** US 8,035,112 B1
(45) **Date of Patent:** Oct. 11, 2011

(54) **SIC POWER DMOSFET WITH
SELF-ALIGNED SOURCE CONTACT**

(75) Inventors: **James A. Cooper**, West Lafayette, IN
(US); **Asmita Saha**, Hillsboro, OR (US)

(73) Assignee: **Purdue Research Foundation**, West
Lafayette, IN (US)

(*) Notice: Subject to any disclaimer, the term of this
patent is extended or adjusted under 35
U.S.C. 154(b) by 91 days.

(21) Appl. No.: 12/429,176

(22) Filed: Apr. 23, 2009

Related U.S. Application Data

(60) Provisional application No. 61/047,274, filed on Apr.
23, 2008.

(51) **Int. Cl.**
H01L 21/0312 (2006.01)

(52) **U.S. Cl.** 257/77; 257/76; 438/142

(58) **Field of Classification Search** 257/76;
257/77; E21D05; 438/105; 142
See application file for complete search history.

(56) **References Cited**

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5,780,324 A 7/1998 Tokura et al.
5,786,251 A 7/1998 Harris et al.
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6,150,671 A 11/2000 Harris et al.
6,180,958 B1 1/2001 Cooper
6,238,980 B1 5/2001 Ueno

6,297,100 B1 10/2001 Kumar et al.
6,316,906 B1 11/2001 Mo
6,344,663 B1 2/2002 Slater et al.
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6,465,807 B1 10/2002 Ueno
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U.S. Appl. No. 12/429,153, filed Apr. 23, 2009, Cooper et al.
B. Jayar Baliga, "Power Semiconductor Devices," PWS Publishing
Co., 1996, Ch. 7, "Power MOSFET," pp. 335-421.

(Continued)

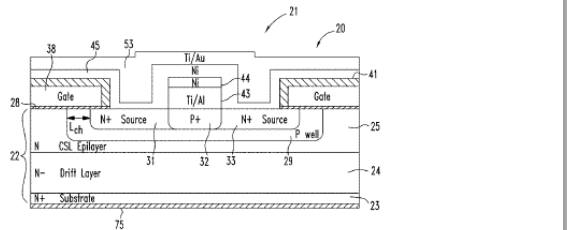
Primary Examiner — Phuc Dang
(74) *Attorney, Agent, or Firm* — William F. Bahret; R.
Randall Frisk

(57)

ABSTRACT

An intermediate product in the fabrication of a MOSFET,
including a silicon carbide wafer having a substrate and a drift
layer on said substrate, said drift layer having a plurality of
source regions formed adjacent an upper surface thereof; a
first oxide layer on said upper surface of said drift layer; a
plurality of polysilicon gates above said first oxide layer, said
plurality of polysilicon gates including a first gate adjacent a
first of said source regions; an oxide layer over said first
source region of greater thickness than said first oxide layer;
and, an oxide layer over said first gate of substantially greater
thickness than said oxide layer over said first source region.

16 Claims, 5 Drawing Sheets



Title: SIC POWER DMOSFET WITH SELF-ALIGNED SOURCE CONTACT

Priority Date: April 23, 2008

Filed Date: April 23, 2009

Issued Date: October 11, 2011

Expiration Date: July 23, 2029

Inventors: James A. Cooper; Asmita Saha

Exemplary Claim: 1


Claim 1

A **silicon carbide power MOSFET**, comprising:

- a **(SUB) silicon carbide wafer having a substrate** and a **(DFT) drift layer** on said **substrate**, said **(DFT) drift layer** having a **(SR) plurality of source regions formed adjacent** an **(US) upper surface** thereof;
- a **(GAT) plurality of polysilicon gates above** said **(DFT) drift layer**, said **(GAT) plurality of polysilicon gates** including a **(GAT1) first gate** adjacent a **(SR1) first of said source regions**,
- said **(GAT1) first gate** having a **(TOP) top surface**, a **(BOT) lower surface** and a **(SW) sidewall**, said **(SW) sidewall overlying** said **(SR1) first source region**;
- a **(SOX) first oxide layer between** said **(BOT) first gate lower surface** and said **(US) upper surface** of said **(DFT) drift layer**;
- a **(ILD) second, thicker oxide layer** over said **(TOP) top surface** and **(SW) sidewall** of said **(GAT1) first gate**;
- and
- a **(ML) conformal layer of metal** extending laterally across said **(GAT1) first gate (TOP) top surface** and **(SW) sidewall** and said **adjacent (SR1) first source region**.

Claim 1

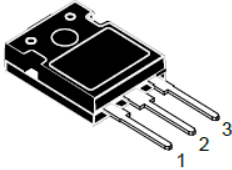
A **silicon carbide power MOSFET**, comprising:



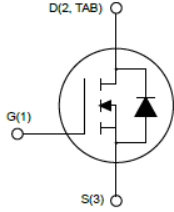
SCTW70N120G2V

Datasheet

Silicon carbide Power MOSFET 1200 V, 91 A, 21 mΩ (typ., T_J = 25 °C)
in an HiP247 package



HiP247



AM01475v1_no2en

Features

Order code	V _{DS}	R _{DS(on)} typ.	I _D
SCTW70N120G2V	1200 V	21 mΩ	91 A

- Very high operating junction temperature capability (T_J = 200 °C)
- Very fast and robust intrinsic body diode
- Extremely low gate charge and input capacitances

Applications

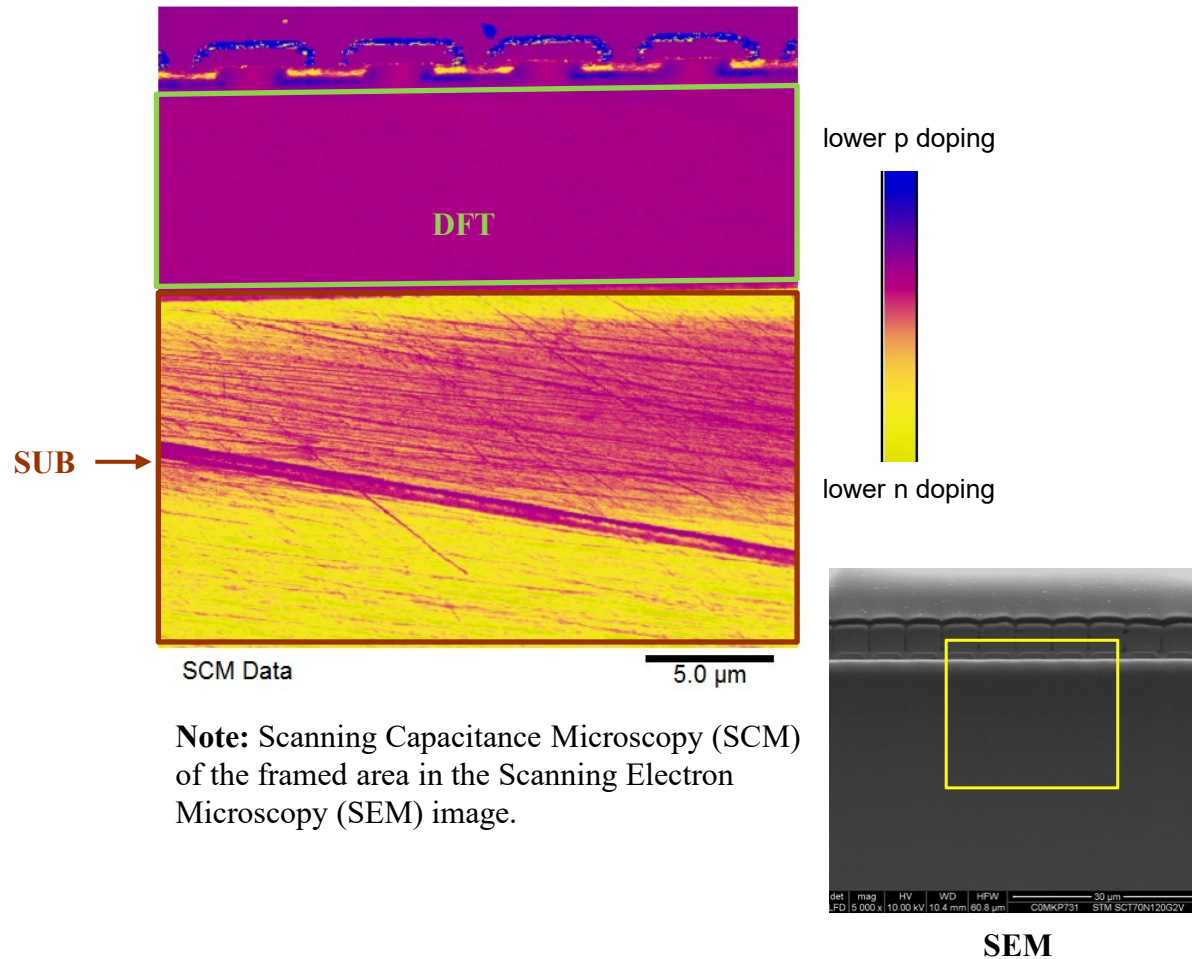
- Charger
- Power supply for renewable energy systems
- High frequency DC-DC converters

Description

This silicon carbide Power MOSFET is produced exploiting the advanced, innovative properties of wide bandgap materials. This results in unsurpassed on-resistance per unit area and very good switching performance almost independent of temperature. The outstanding thermal properties of the SiC material allow designers to use an industry-standard outline with significantly improved thermal capability. These features render the device perfectly suitable for high-efficiency and high power density applications.

Claim 1

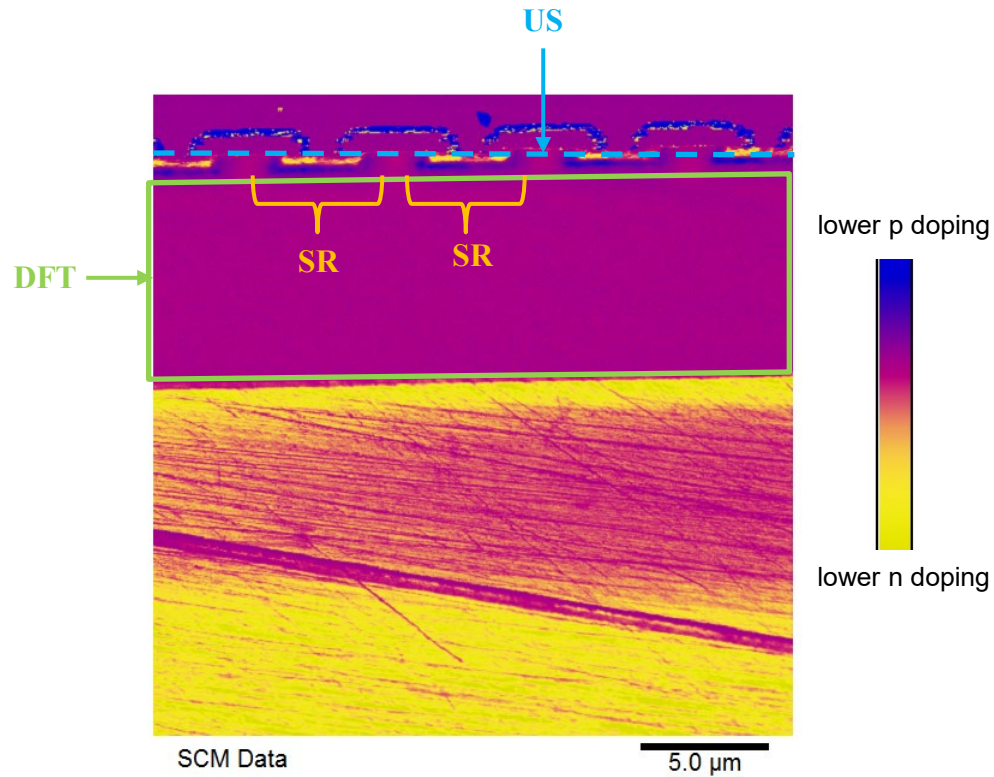
a (SUB) silicon carbide wafer having a substrate and a (DFT) drift layer on said substrate,



Note: Scanning Capacitance Microscopy (SCM) of the framed area in the Scanning Electron Microscopy (SEM) image.

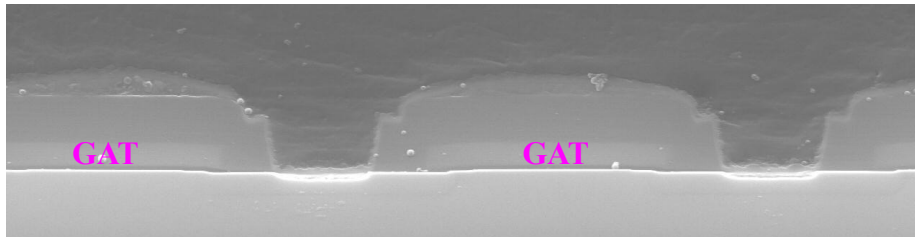
Claim 1

said (DFT) drift layer having a (SR) plurality of source regions formed adjacent an (US) upper surface thereof;

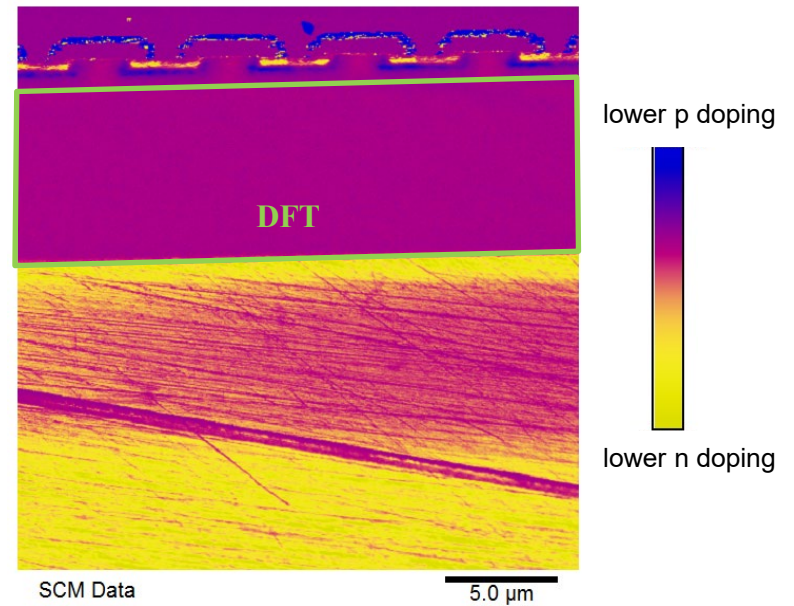


Claim 1

a (GAT) plurality of polysilicon gates above said (DFT) drift layer,

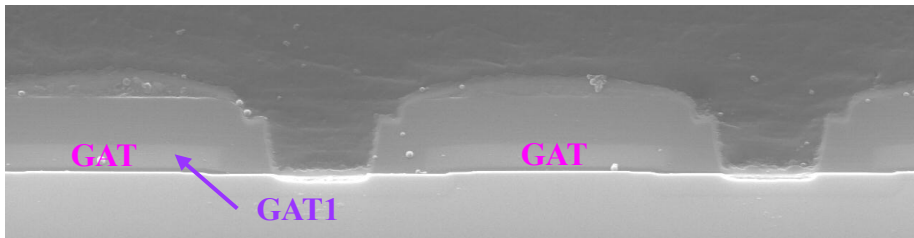


SEM

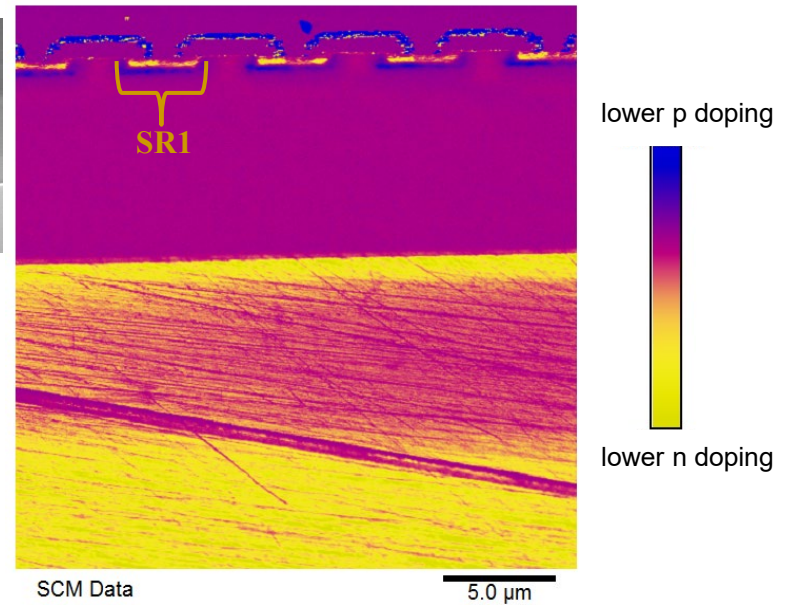


Claim 1

said **(GAT) plurality of polysilicon gates** including a **(GAT1) first gate** adjacent a **(SR1) first of said source regions**,

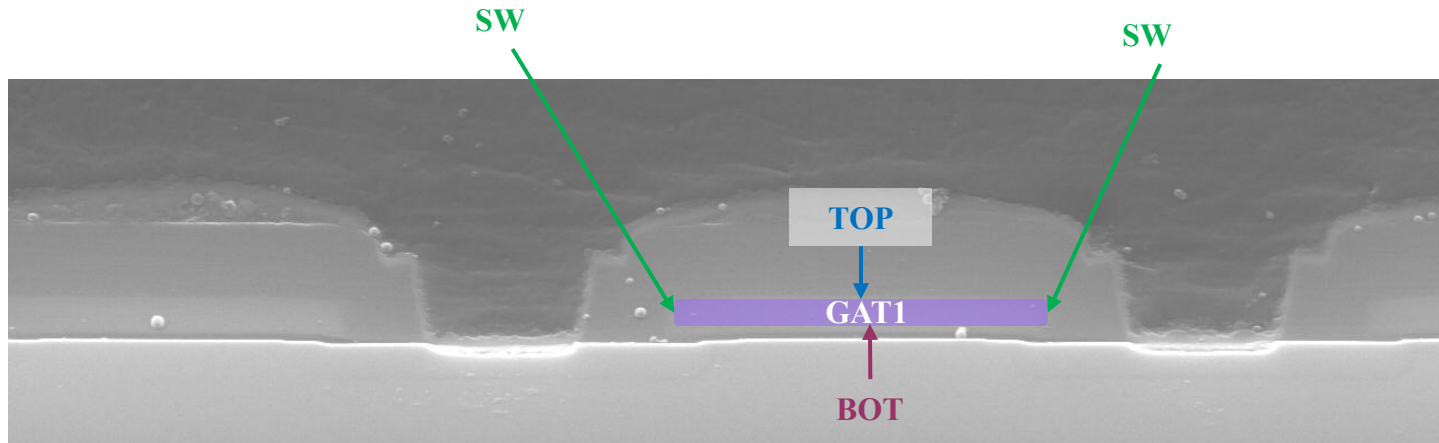


SEM



Claim 1

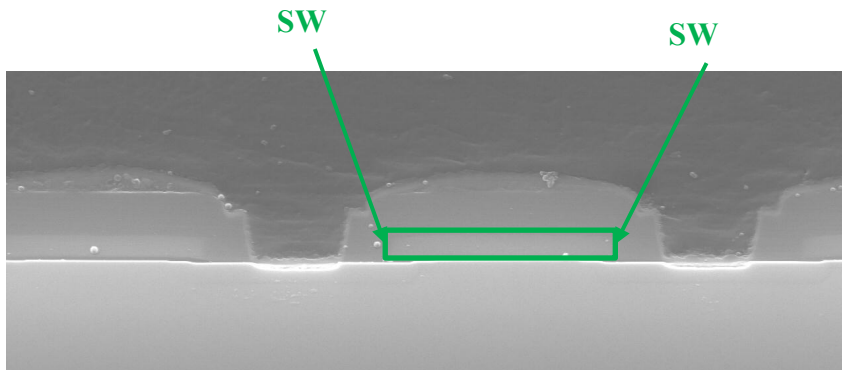
said **(GAT1) first gate** having a **(TOP) top surface**, a **(BOT) lower surface** and a **(SW) sidewall**,



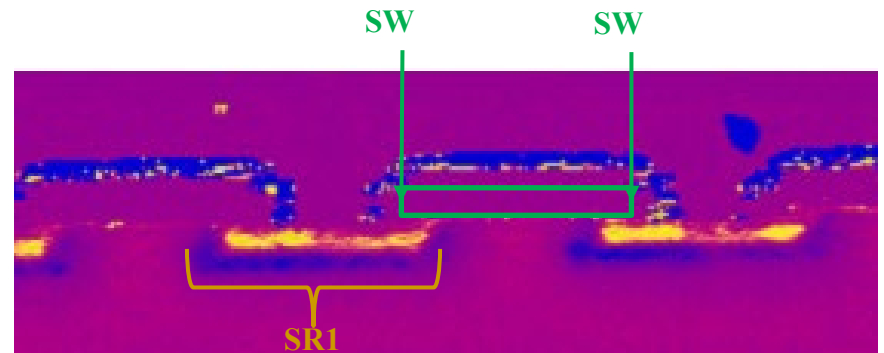
SEM

Claim 1

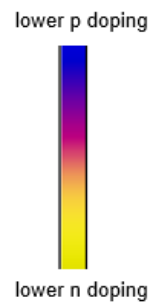
said (SW) sidewall overlying said (SR1) first source region;



SEM

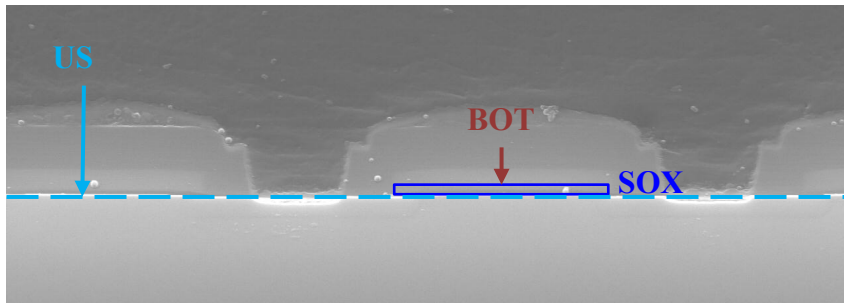


SCM

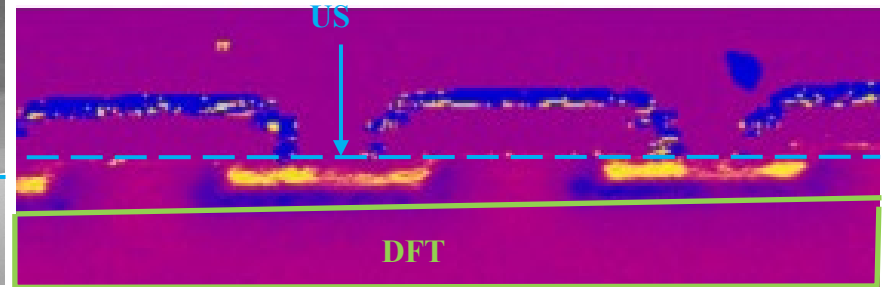


Claim 1

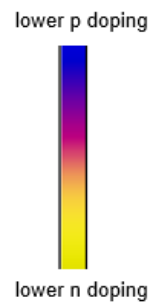
a (SOX) first oxide layer between said (BOT) first gate lower surface and said (US) upper surface of said (DFT) drift layer;



SEM

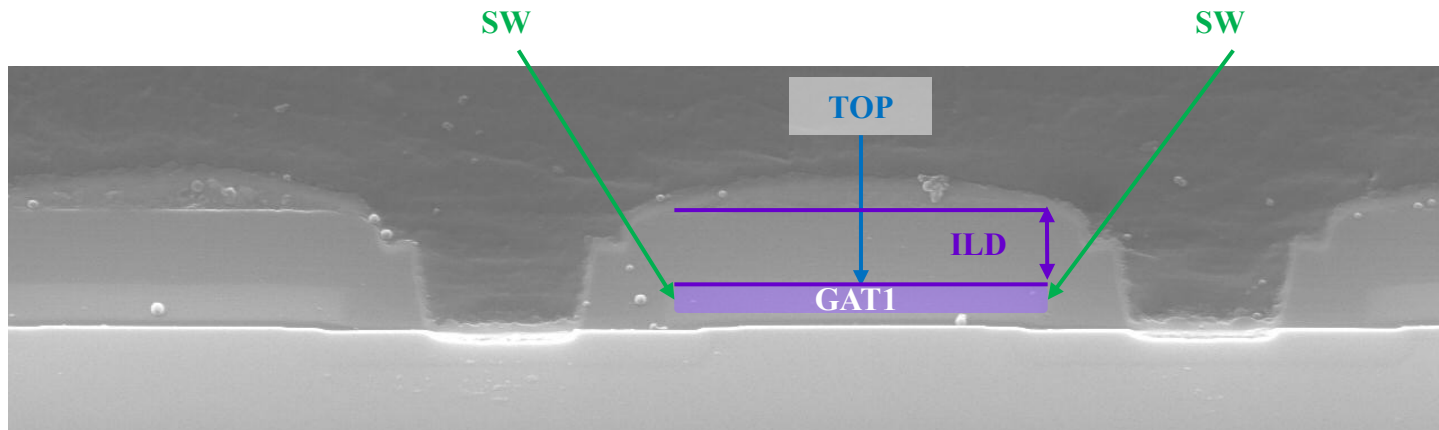


SCM



Claim 1

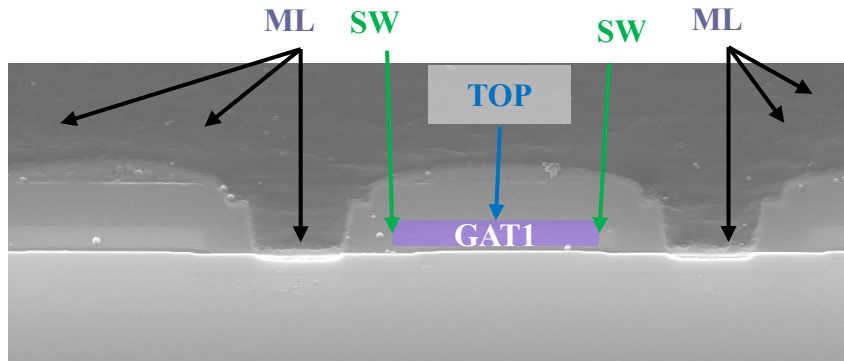
a **(ILD) second, thicker oxide layer** over said **(TOP) top surface** and **(SW) sidewall** of said **(GAT1) first gate**; and



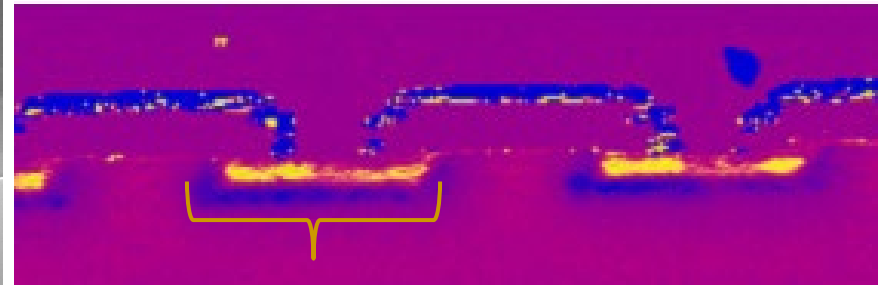
SEM

Claim 1

a (ML) conformal layer of metal extending laterally across said (GAT1) first gate (TOP) top surface and (SW) sidewall and said adjacent (SR1) first source region.




SEM

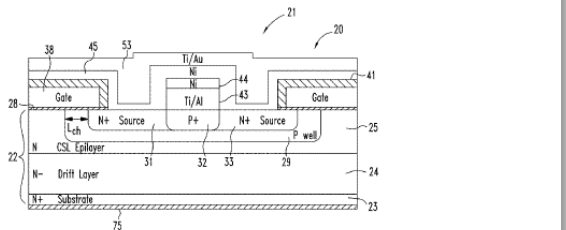


SR1

SCM



	
US008035112B1	
(12) United States Patent Cooper et al.	(10) Patent No.: US 8,035,112 B1 (45) Date of Patent: Oct. 11, 2011
<p>(54) SIC POWER DMOSFET WITH SELF-ALIGNED SOURCE CONTACT</p> <p>(75) Inventors: James A. Cooper, West Lafayette, IN (US); Asmita Saha, Hillsboro, OR (US)</p> <p>(73) Assignee: Purdue Research Foundation, West Lafayette, IN (US)</p> <p>(*) Notice: Subject to any disclaimer, the term of this patent is extended or adjusted under 35 U.S.C. 154(b) by 91 days.</p> <p>(21) Appl. No.: 12/429,176</p> <p>(22) Filed: Apr. 23, 2009</p> <p>Related U.S. Application Data</p> <p>(60) Provisional application No. 61/047,274, filed on Apr. 23, 2008.</p> <p>(51) Int. Cl. H01L 21/0312 (2006.01)</p> <p>(52) U.S. Cl. 257/77; 257/76; 438/142</p> <p>(58) Field of Classification Search 257/76; 257/77; E21/065; 438/105; 142</p> <p>See application file for complete search history.</p> <p>(56) References Cited</p> <p>U.S. PATENT DOCUMENTS</p> <p>4,070,690 A 1/1978 Wickstrom</p> <p>4,893,160 A 1/1990 Blanchard</p> <p>5,506,421 A 4/1996 Palmour</p> <p>5,637,898 A 6/1997 Baliga</p> <p>5,780,324 A 7/1998 Tokura et al.</p> <p>5,786,251 A 7/1998 Harris et al.</p> <p>5,801,417 A 9/1998 Tsang et al.</p> <p>5,814,859 A 9/1998 Chizzola et al.</p> <p>6,054,752 A 4/2000 Han et al.</p> <p>6,150,671 A 11/2000 Harris et al.</p> <p>6,180,958 B1 1/2001 Cooper</p> <p>6,238,980 B1 5/2001 Ueno</p> <p>6,297,100 B1 10/2001 Kumar et al.</p> <p>6,316,906 B1 11/2001 Mo</p> <p>6,344,663 B1 2/2002 Slater et al.</p> <p>6,362,495 B1 3/2002 Schoen et al.</p> <p>6,465,807 B1 10/2002 Ueno</p> <p>6,573,534 B1 * 6/2003 Kumar et al. 257/77</p> <p>6,737,677 B2 5/2004 Shimoda et al. 438/268</p> <p>6,815,293 B2 * 11/2004 Dunne et al. 438/268</p> <p>6,894,319 B2 5/2005 Kobayashi et al.</p> <p>7,074,643 B2 7/2006 Ryu</p> <p>7,498,633 B2 3/2009 Cooper et al.</p> <p>7,521,731 B2 * 4/2009 Shimoda et al. 257/183</p> <p>7,622,741 B2 * 11/2009 Munn 257/77</p> <p>2003/0073,270 A1 * 4/2003 Hosoda et al. 438/197</p> <p>2004/0145011 A1 7/2004 Imai et al.</p> <p>2006/0065925 A1 3/2006 Yoshida</p> <p>2007/0209968 A1 11/2007 Saxler et al.</p> <p>OTHER PUBLICATIONS</p> <p>U.S. Appl. No. 10/821,613, filed Apr. 9, 2004, Cooper et al.</p> <p>U.S. Appl. No. 12/429,153, filed Apr. 23, 2009, Cooper et al.</p> <p>B. Jayar Baliga, "Power Semiconductor Devices," PWS Publishing Co., 1996, Ch. 7, "Power MOSFET," pp. 335-421.</p> <p>(Continued)</p> <p>Primary Examiner — Phuc Dang (74) Attorney, Agent, or Firm — William F. Bahret; R. Randall Frisk</p> <p>(57) ABSTRACT</p> <p>An intermediate product in the fabrication of a MOSFET, including a silicon carbide wafer having a substrate and a drift layer on said substrate, said drift layer having a plurality of source regions formed adjacent an upper surface thereof; a first oxide layer on said upper surface of said drift layer; a plurality of polysilicon gates above said first oxide layer, said plurality of polysilicon gates including a first gate adjacent a first of said source regions; an oxide layer over said first source region of greater thickness than said first oxide layer; and, an oxide layer over said first gate of substantially greater thickness than said oxide layer over said first source region.</p> <p>16 Claims, 5 Drawing Sheets</p>	



Title: SIC POWER DMOSFET WITH SELF-ALIGNED SOURCE CONTACT

Priority Date: April 23, 2008

Filed Date: April 23, 2009

Issued Date: October 11, 2011

Expiration Date: July 23, 2029

Inventors: James A. Cooper; Asmita Saha

Exemplary Claims: 6, 7, 10, 11, 12

Claim 6

A **mosfet structure**, comprising:

a **(SUB) silicon carbide wafer having a substrate body** with an **(US) upper surface**,
said **(SUB) substrate body** having **(SR) at least one source region** formed **(US) adjacent said upper surface**;
a **(SOX) substrate surface oxidation layer** on said **(US) upper surface** of said **(SUB) substrate body** and **(SR) adjacent said source region**;
(GAT) at least two polysilicon gates above said **(SOX) substrate surface oxidation layer**, said **(GAT) gates**
each having a **(TOP) top**, a **(BOT) bottom** and **(SID) sides**, wherein a **(SR) first source region of said at least one source region** is juxtaposed between **(GAT) first and second adjacent gates of said at least two polysilicon gates**;
a **(ILD) gate oxide layer**, thicker than said **(SOX) substrate surface oxidation layer**, over said **(TOP) tops** and **(SID) sides** of **(GAT) each of said gates**; and
a **(ML) material layer** over said **(SR) first source region** and between said **(ILD) gate oxide layers** on said **(SID) sides** of said **(GAT) gates**,
said **(ML) material layer** comprising one of an oxide and a **(ML) metal contact**.

Claim 7

The **mosfet structure** of claim 6, wherein said **(ILD) gate oxide layer** is more than **(I) eight times thicker** than said **(SOX) substrate surface oxidation layer**.

Claim 10

The **MOSFET structure** of claim 6, wherein said **(ML) material layer is a metal contact layer providing external electrical contact with** said at least one **(SR) source region**.

Claim 11


The **MOSFET structure** of claim 10 wherein said **(ML) metal contact layer extends over substantially the entire MOSFET structure except for at least one (GC) gate contact access portion**, said **(ML) metal contact layer being in electrical contact with** said **at least one (SR) source region** but **electrically insulated from said at least two (GAT) polysilicon gates by** at least one of said **(ILD) gate oxide layer** and said substrate surface oxidation layer.

Claim 12

The **MOSFET structure** of claim 10, wherein said **(ML) metal contact layer extends over said (GAT) gates and covers the space between them**, said **(ML) metal contact layer being in electrical contact with** said **at least one (SR) source region** but **electrically insulated from said (GAT) gates by** at least one of said **(ILD) gate oxide layer** and said substrate surface oxidation layer.

Claim 6

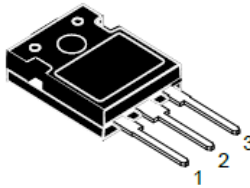
A **MOSFET structure**, comprising:



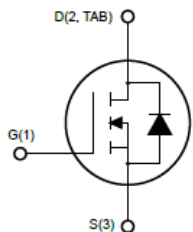
SCTW90N65G2V

Datasheet

**Silicon carbide Power MOSFET 650 V, 119 A, 18 mΩ (typ., T_J = 25 °C)
in an HiP247 package**



HiP247



AIM01475v1_no2en

Features

Order code	V _{DS}	R _{DS(on)} max.	I _D
SCTW90N65G2V	650 V	24 mΩ	119 A

- Very high operating junction temperature capability (T_J = 200 °C)
- Very fast and robust intrinsic body diode
- Extremely low gate charge and input capacitances

Applications

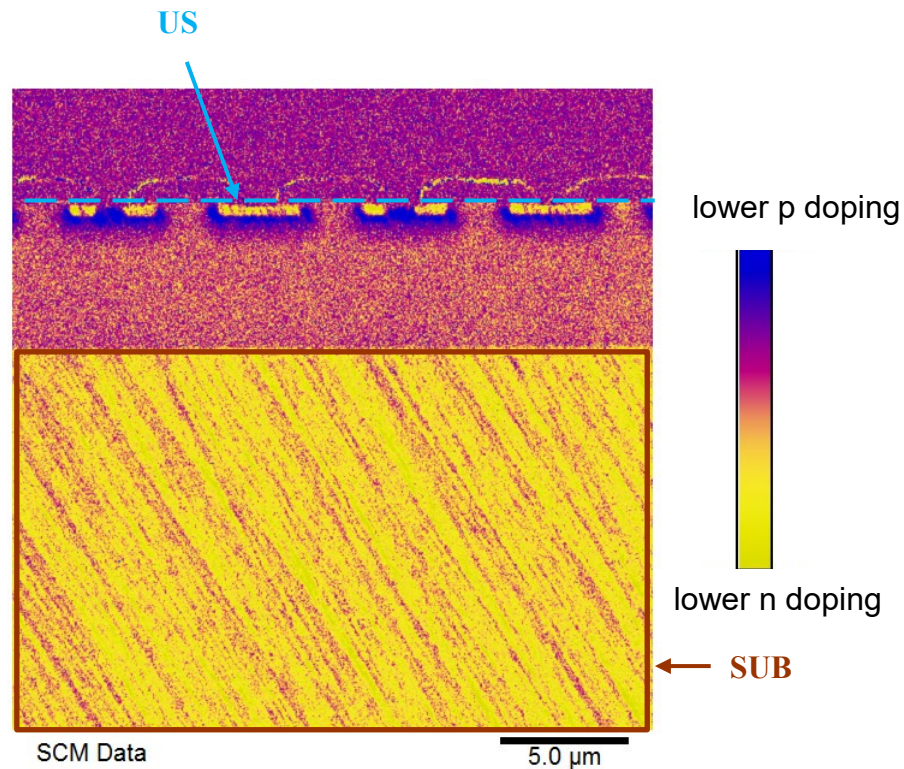
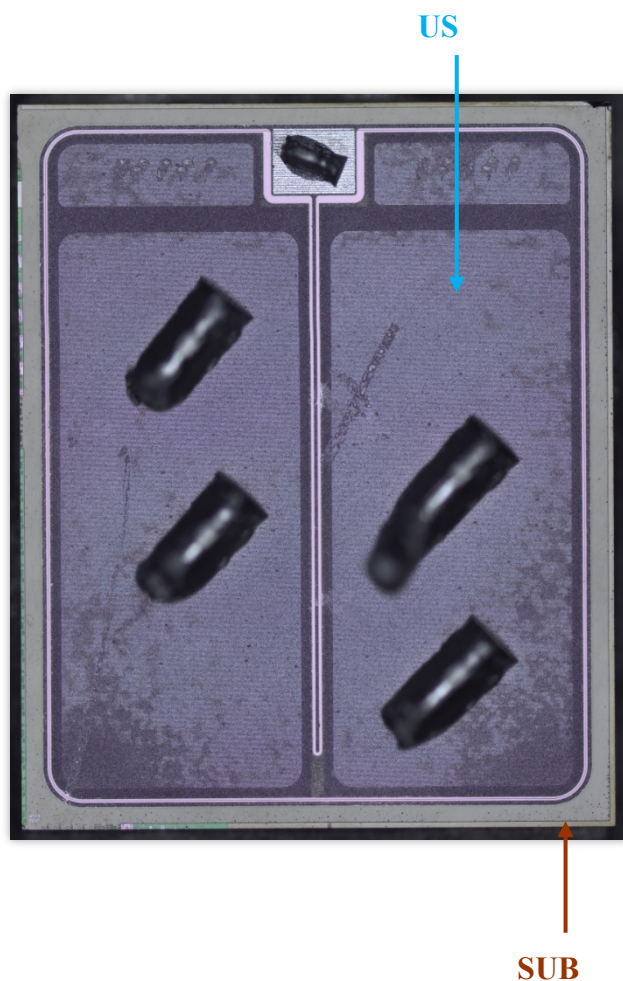
- Switching applications
- Power supply for renewable energy systems
- High frequency DC-DC converters

Description

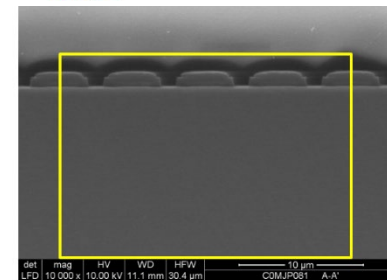
This silicon carbide Power MOSFET device has been developed using ST's advanced and innovative 2nd generation SiC MOSFET technology. The device features remarkably low on-resistance per unit area and very good switching performance. The variation of switching loss is almost independent of junction temperature.

Claim 6

a (SUB) silicon carbide wafer having a substrate body with an (US) upper surface,



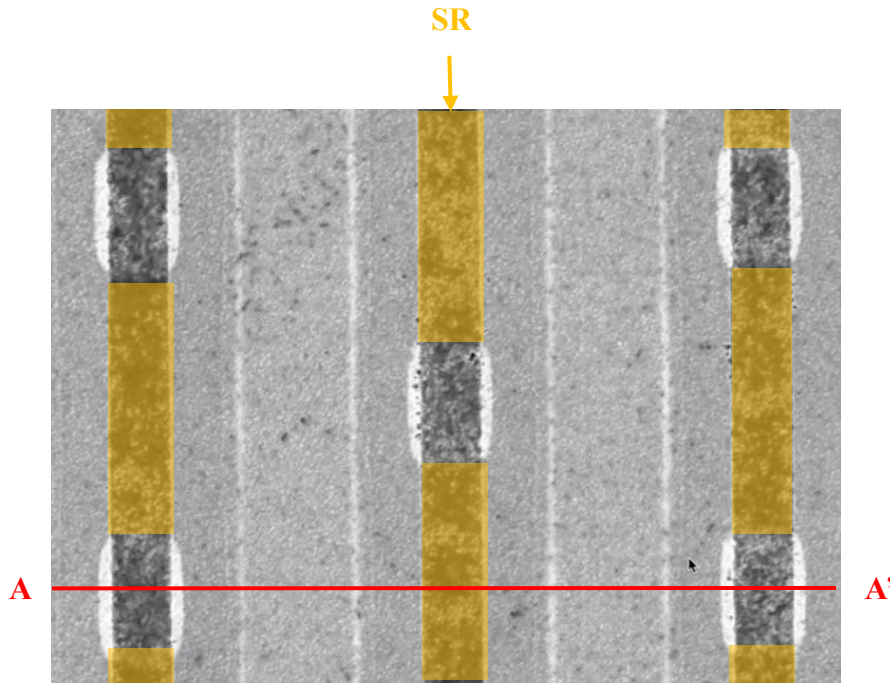
Note: Scanning Capacitance Microscopy (SCM) of the framed area in the Scanning Electron Microscopy (SEM) image.



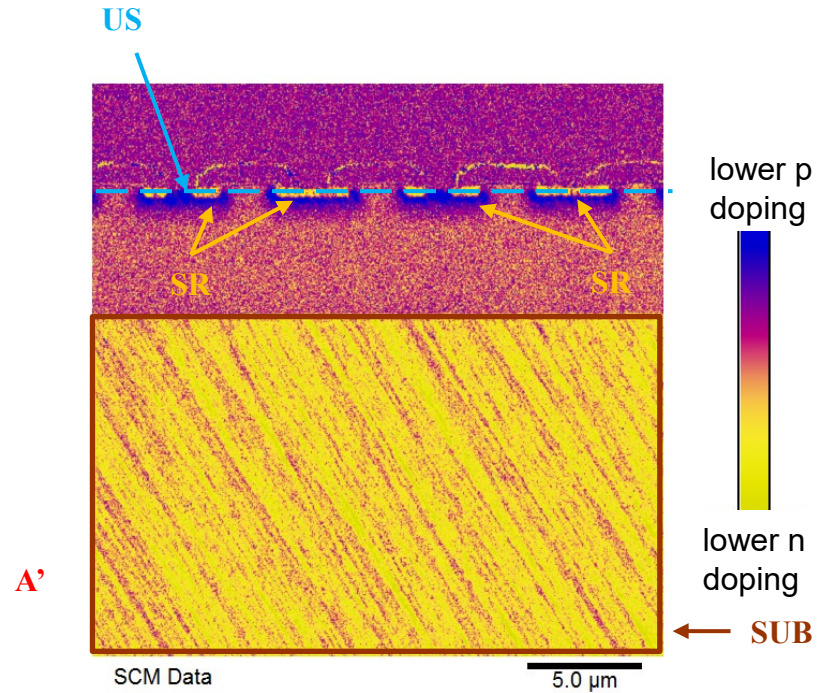
SEM

Claim 6

said (SUB) substrate body having (SR) at least one source region formed (US) adjacent said upper surface;



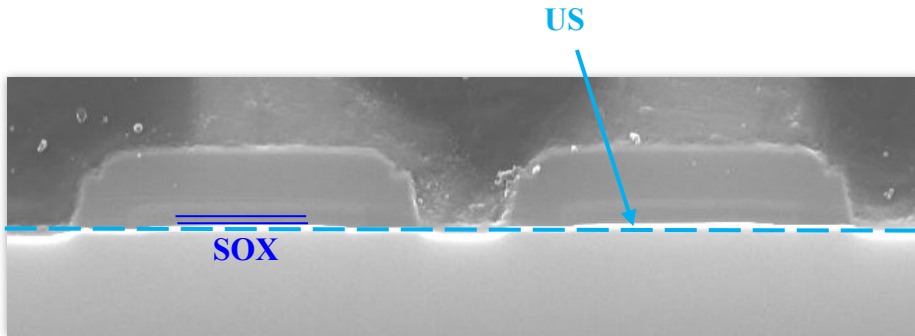
Note: Top-down view using Scanning Electron Microscopy Secondary Electron Potential Contrast (SEM SEPC), after polishing down to the silicon carbide.



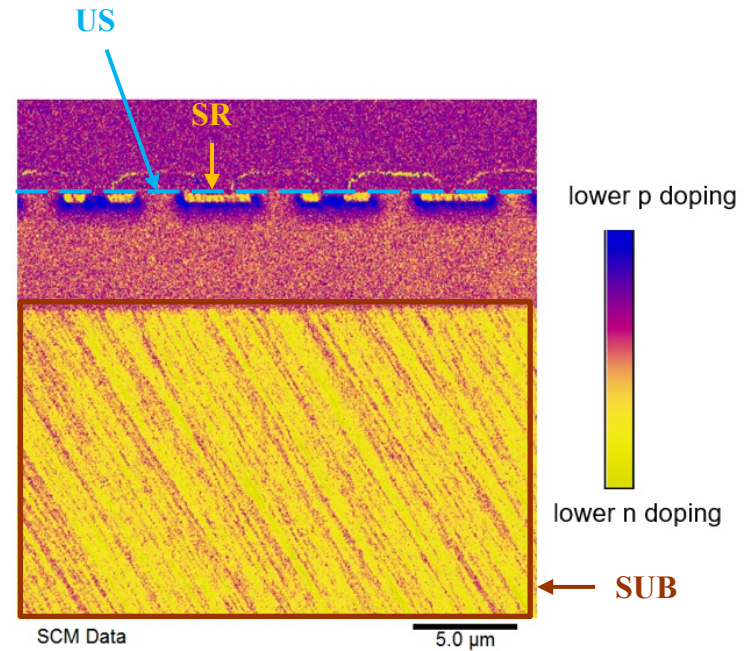
Note: SCM view taken at A-A' cross section

Claim 6

a **(SOX) substrate surface oxidation layer** on said **(US) upper surface** of said **(SUB) substrate body** and **(SR) adjacent said source region**;

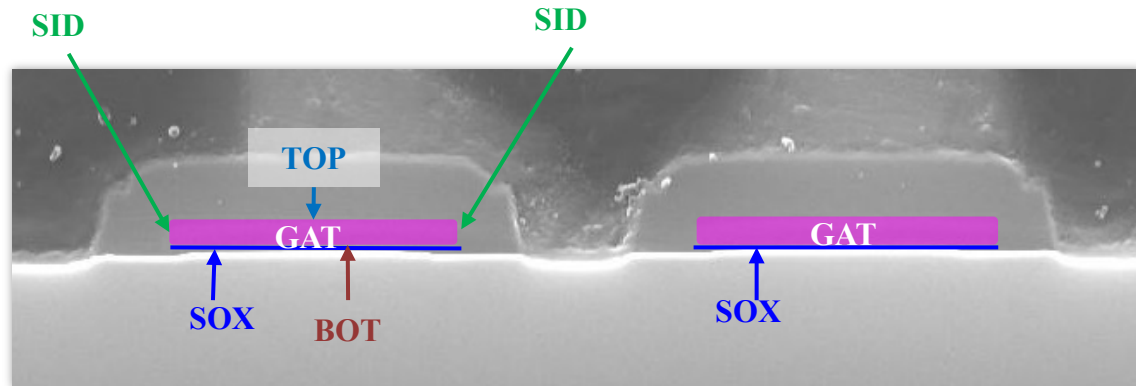


SEM



Claim 6

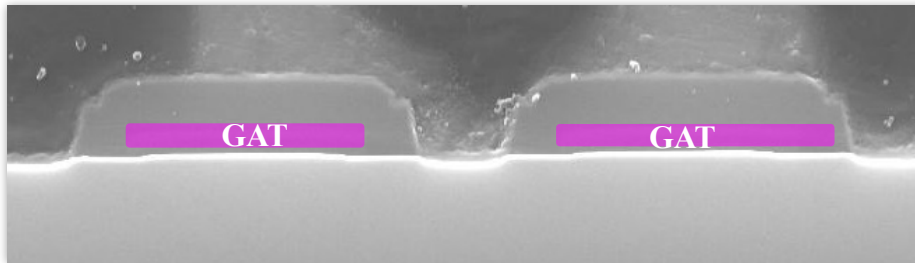
(GAT) at least two polysilicon gates above said (SOX) substrate surface oxidation layer, said (GAT) gates each having a (TOP) top, a (BOT) bottom and (SID) sides,



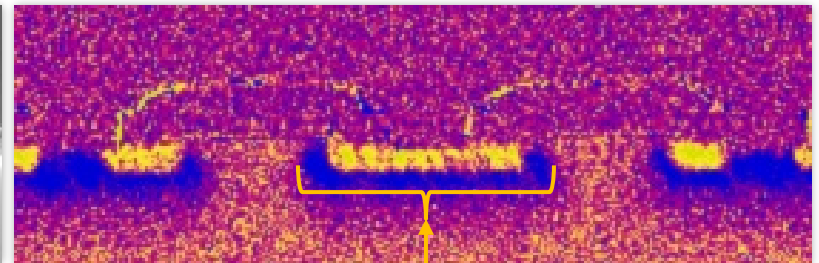
SEM

Claim 6

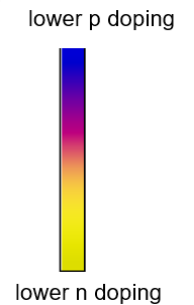
wherein a (SR) first source region of said at least one source region is juxtaposed between (GAT) first and second adjacent gates of said at least two polysilicon gates;



SEM

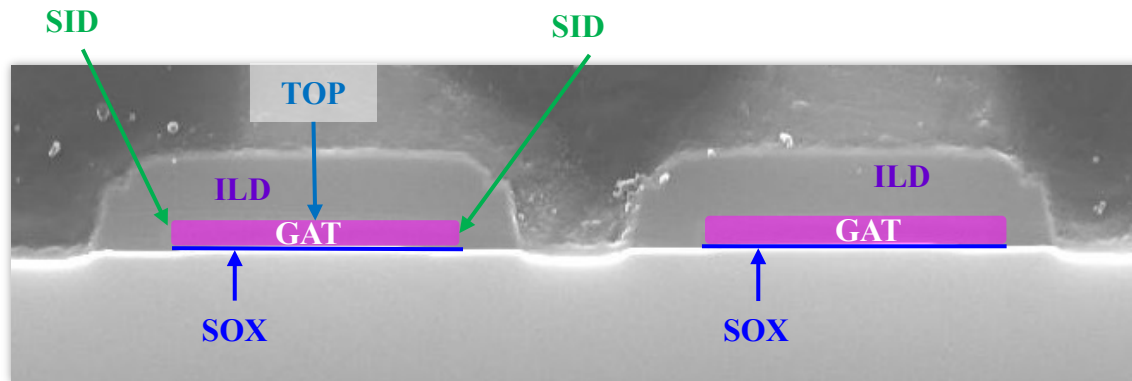


SR
SCM



Claim 6

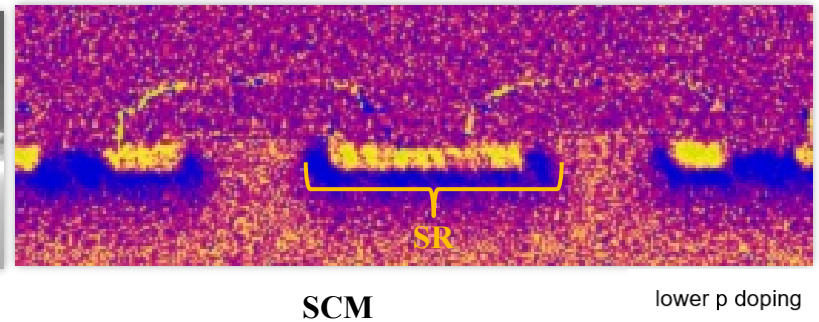
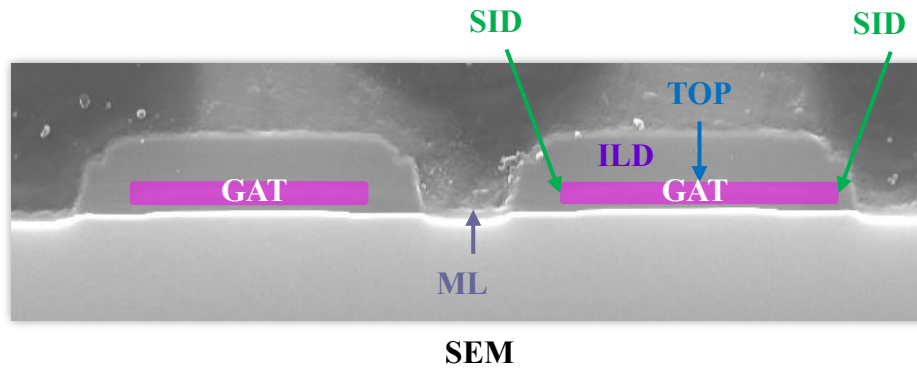
a **(ILD) gate oxide layer**, thicker than said **(SOX) substrate surface oxidation layer**, over said **(TOP) tops** and **(SID) sides** of **(GAT) each of said gates**; and



SEM

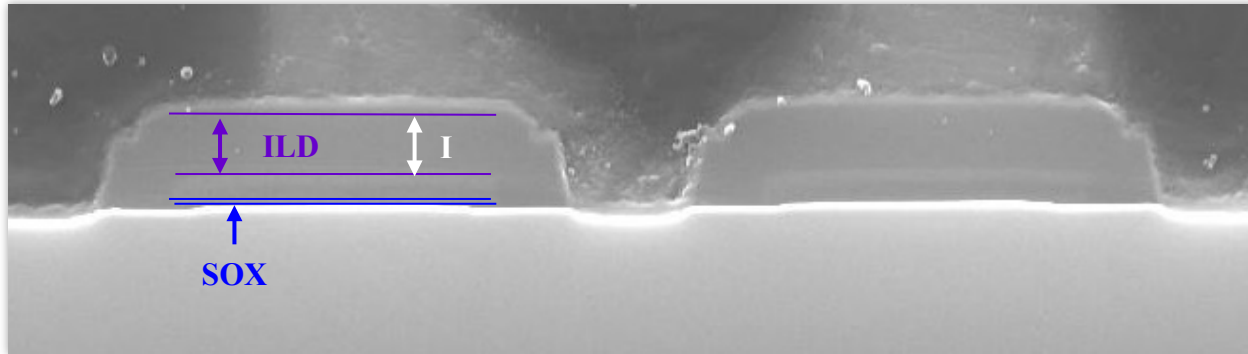
Claim 6

a (ML) material layer over said (SR) first source region and between said (ILD) gate oxide layers on said (SID) sides of said (GAT) gates, said (ML) material layer comprising one of an oxide and a (ML) metal contact.



Claim 7

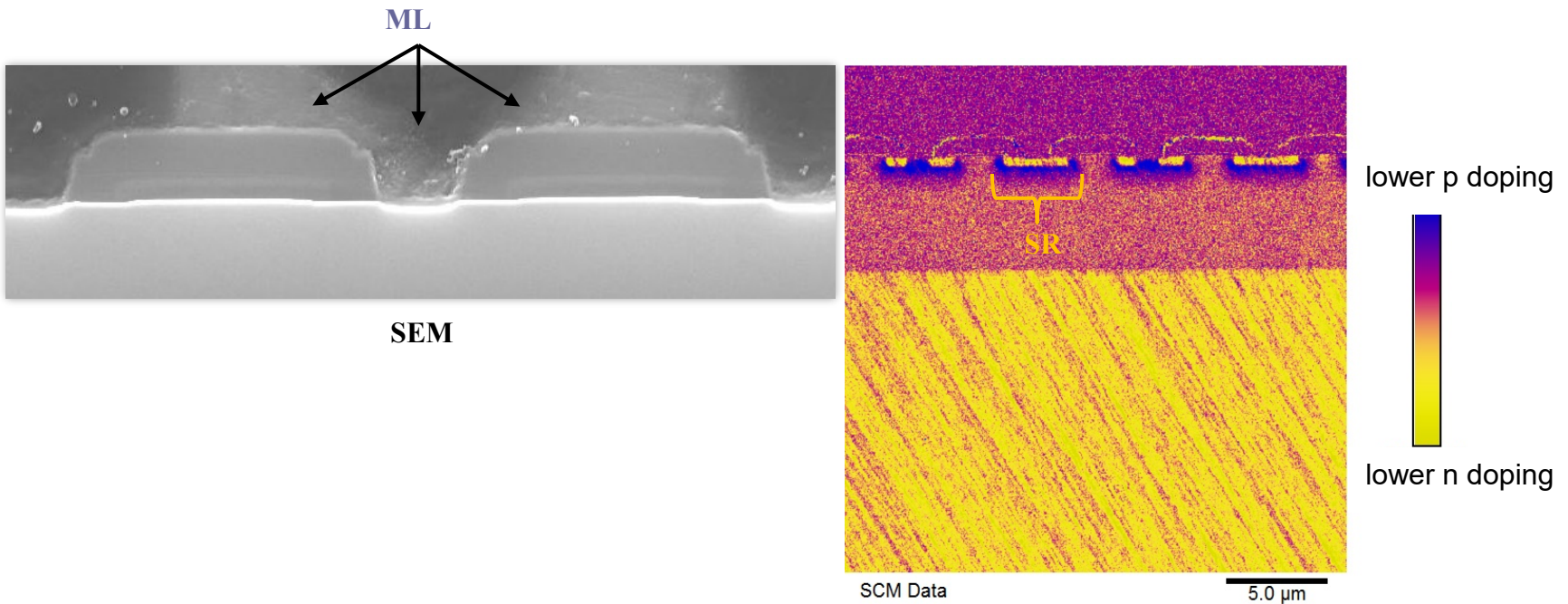
The mosfet structure of claim 6, wherein said **(ILD) gate oxide layer** is more than **(I) eight times thicker** than said **(SOX) substrate surface oxidation layer**.



SEM

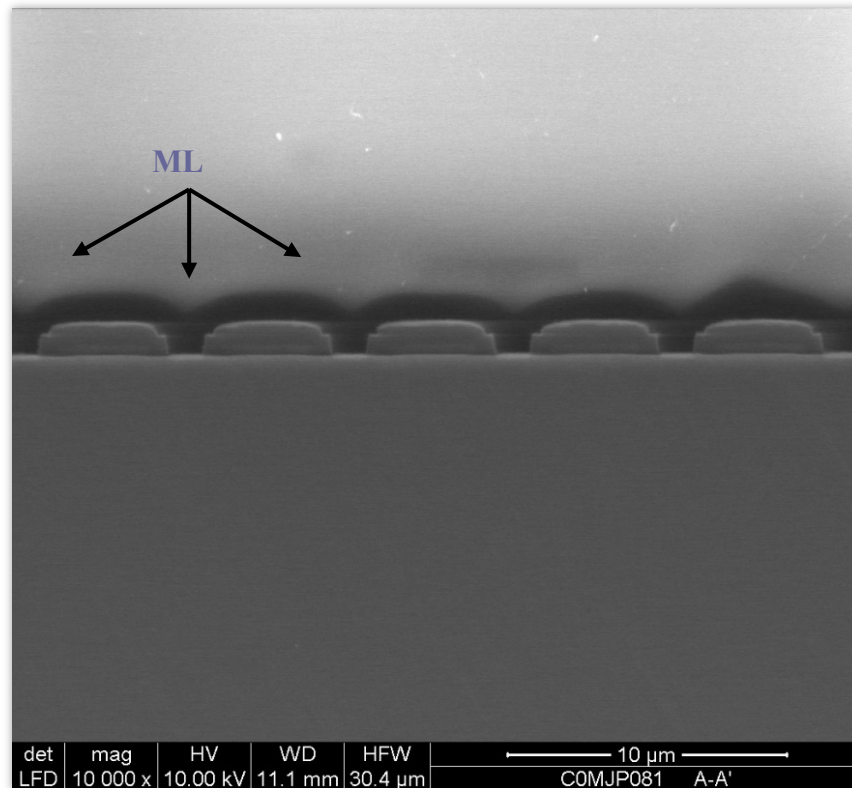
Claim 10

The **MOSFET structure** of claim 6, wherein said **(ML) material layer** is a metal contact layer providing external electrical contact with said at least one **(SR) source region**.



Claim 11

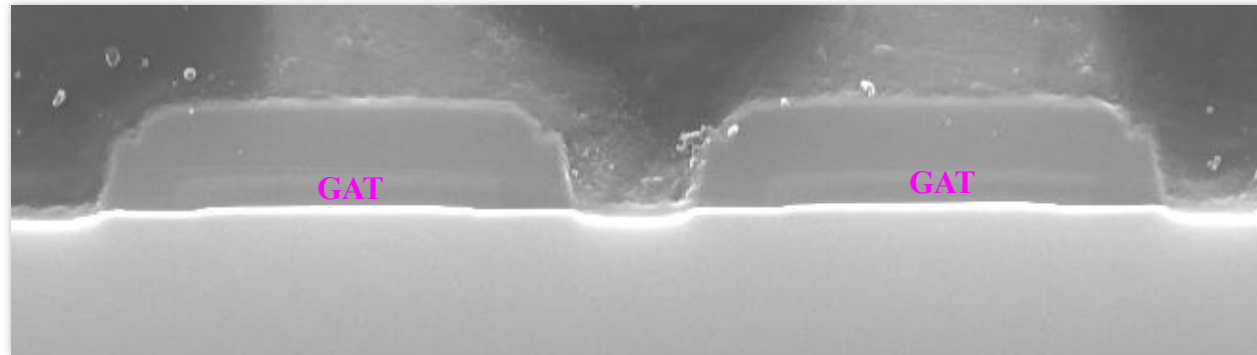
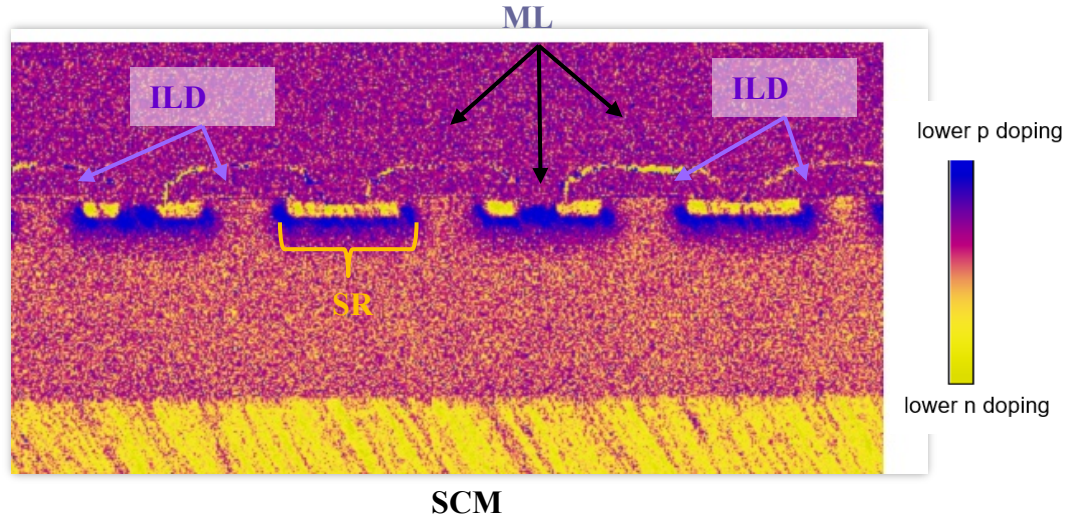
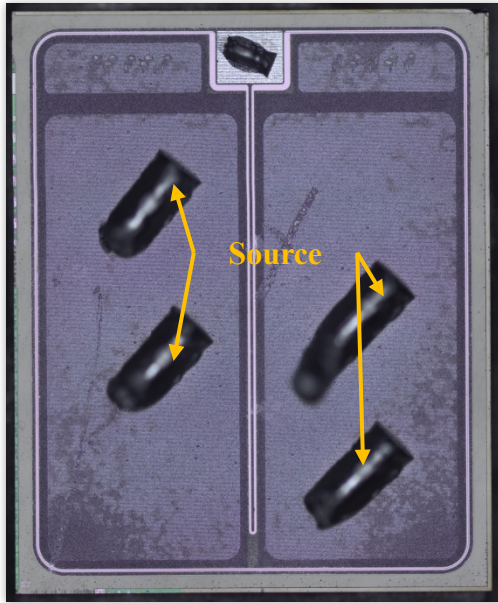
The **MOSFET structure** of claim 10 wherein said **(ML) metal contact layer** extends over substantially the entire MOSFET structure except for at least one **(GC) gate contact access portion**,



SEM

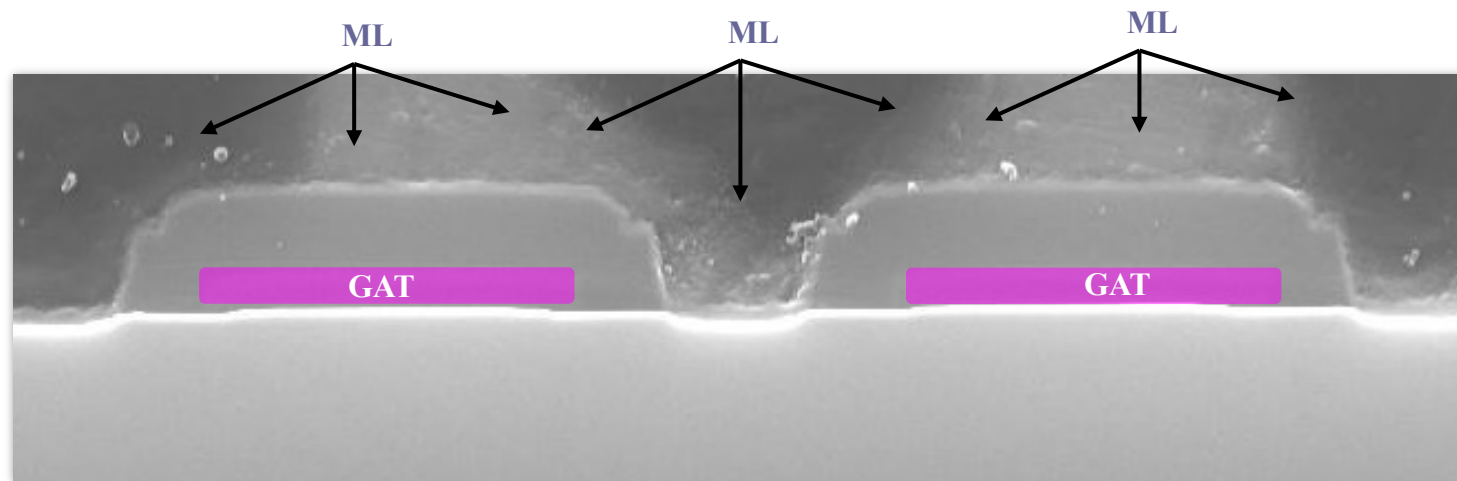
Claim 11

said (ML) metal contact layer being in electrical contact with said **at least one (SR) source region** but **electrically insulated from said at least two (GAT) polysilicon gates by** at least one of said (ILD) gate oxide layer and said substrate surface oxidation layer.



Claim 12

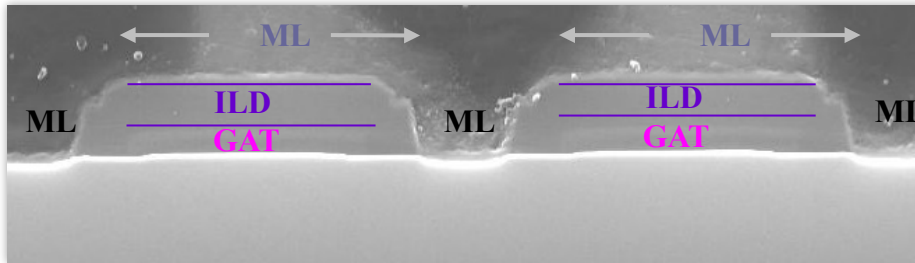
The **MOSFET structure** of claim 10, wherein said **(ML) metal contact layer** extends over said **(GAT) gates** and covers the space between them,



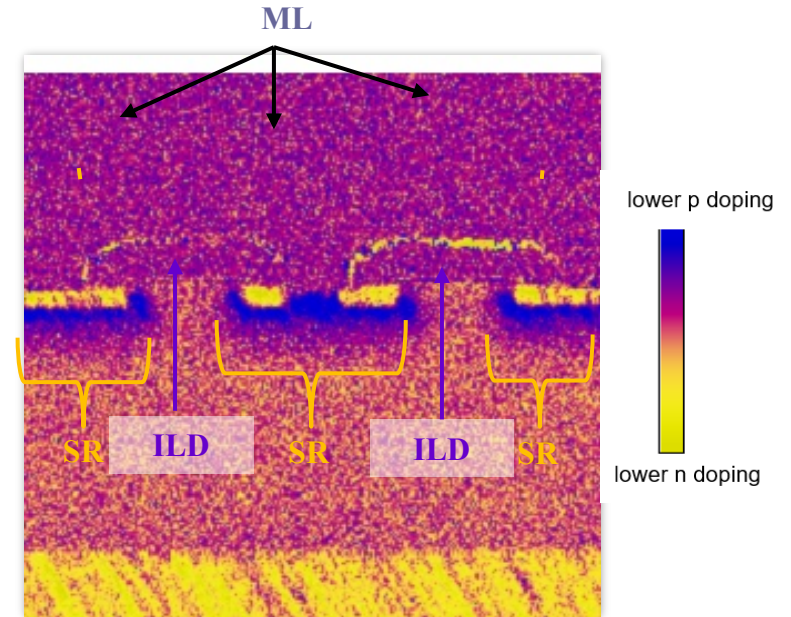
SEM

Claim 12

said (ML) metal contact layer being in electrical contact with said at least one (SR) source region but electrically insulated from said (GAT) gates by at least one of said (ILD) gate oxide layer and said substrate surface oxidation layer.



SEM



SCM



US008035112B1

(12) **United States Patent**
Cooper et al.

(10) **Patent No.:** US 8,035,112 B1
(45) **Date of Patent:** Oct. 11, 2011

- (54) **SIC POWER DMOSFET WITH SELF-ALIGNED SOURCE CONTACT**
- (75) Inventors: **James A. Cooper**, West Lafayette, IN (US); **Asmita Saha**, Hillsboro, OR (US)
- (73) Assignee: **Purdue Research Foundation**, West Lafayette, IN (US)
- (*) Notice: Subject to any disclaimer, the term of this patent is extended or adjusted under 35 U.S.C. 154(b) by 91 days.
- (21) Appl. No.: **12/429,176**
- (22) Filed: **Apr. 23, 2009**

Related U.S. Application Data

- (60) Provisional application No. 61/047,274, filed on Apr. 23, 2008.
- (51) **Int. Cl.** **H01L 21/0312** (2006.01)
- (52) **U.S. Cl.** 257/77; 257/76; 438/142
- (58) **Field of Classification Search** 257/76; 257/77; E21D065; 438/105; 142
- See application file for complete search history.

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6,150,671 A 11/2000 Harris et al.
6,180,958 B1 1/2001 Cooper
6,238,980 B1 5/2001 Ueno

U.S. Appl. No. 10/821,613, filed Apr. 9, 2004, Cooper et al.
U.S. Appl. No. 12/429,153, filed Apr. 23, 2009, Cooper et al.
B. Jayar Baliga, "Power Semiconductor Devices," PWS Publishing Co., 1996, Ch. 7, "Power MOSFET," pp. 335-421.

(Continued)

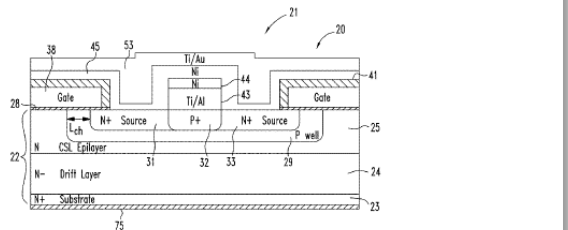
Primary Examiner — Phuc Dung

(74) *Attorney, Agent, or Firm* — William F. Bahret; R. Randall Frisk

(57) **ABSTRACT**

An intermediate product in the fabrication of a MOSFET, including a silicon carbide wafer having a substrate and a drift layer on said substrate, said drift layer having a plurality of source regions formed adjacent an upper surface thereof; a first oxide layer on said upper surface of said drift layer; a plurality of polysilicon gates above said first oxide layer, said plurality of polysilicon gates including a first gate adjacent a first of said source regions; an oxide layer over said first source region of greater thickness than said first oxide layer; and, an oxide layer over said first gate of substantially greater thickness than said oxide layer over said first source region.

16 Claims, 5 Drawing Sheets



Title: SIC POWER DMOSFET WITH SELF-ALIGNED SOURCE CONTACT

Priority Date: April 23, 2008

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Expiration Date: July 23, 2029

Inventors: James A. Cooper; Asmita Saha

Exemplary Claims: 6, 7, 10, 11, 12

Claim 6

A **mosfet structure**, comprising:

- a **(SUB) silicon carbide wafer having a substrate body** with an **(US) upper surface**,
said **(SUB) substrate body** having **(SR) at least one source region** formed **(US) adjacent said upper surface**;
a **(SOX) substrate surface oxidation layer** on said **(US) upper surface** of said **(SUB) substrate body** and **(SR) adjacent said source region**;
- (GAT) at least two polysilicon gates** above said **(SOX) substrate surface oxidation layer**, said **(GAT) gates**
each having a **(TOP) top**, a **(BOT) bottom** and **(SID) sides**, wherein a **(SR) first source region of said at least one source region** is juxtaposed between **(GAT) first and second adjacent gates of said at least two polysilicon gates**;
- a **(ILD) gate oxide layer**, thicker than said **(SOX) substrate surface oxidation layer**, over said **(TOP) tops** and **(SID) sides** of **(GAT) each of said gates**; and
- a **(ML) material layer** over said **(SR) first source region** and between said **(ILD) gate oxide layers** on said **(SID) sides** of said **(GAT) gates**,
said **(ML) material layer** comprising one of an oxide and a **(ML) metal contact**.

Claim 7

The **mosfet structure** of claim 6, wherein said **(ILD) gate oxide layer** is more than **(I) eight times thicker** than said **(SOX) substrate surface oxidation layer**.

Claim 10

The **MOSFET structure** of claim 6, wherein said **(ML) material layer is a metal contact layer providing external electrical contact with** said at least one **(SR) source region**.

Claim 11


The **MOSFET structure** of claim 10 wherein said **(ML) metal contact layer extends over substantially the entire MOSFET structure except for at least one (GC) gate contact access portion**, said **(ML) metal contact layer being in electrical contact with** said **at least one (SR) source region** but **electrically insulated from said at least two (GAT) polysilicon gates by** at least one of said **(ILD) gate oxide layer** and said substrate surface oxidation layer.

Claim 12

The **MOSFET structure** of claim 10, wherein said **(ML) metal contact layer extends over said (GAT) gates and covers the space between them**, said **(ML) metal contact layer being in electrical contact with** said **at least one (SR) source region** but **electrically insulated from said (GAT) gates by** at least one of said **(ILD) gate oxide layer** and said substrate surface oxidation layer.

Claim 6

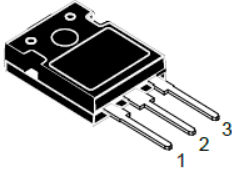
A **MOSFET structure**, comprising:

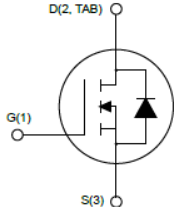
 life.augmented

SCTW70N120G2V

Datasheet

Silicon carbide Power MOSFET 1200 V, 91 A, 21 m Ω (typ., $T_J = 25^\circ\text{C}$)
in an HiP247 package


HiP247


AMD1475v1_no2en

Features

Order code	V_{DS}	$R_{DS(on)}$ typ.	I_D
SCTW70N120G2V	1200 V	21 m Ω	91 A

- Very high operating junction temperature capability ($T_J = 200^\circ\text{C}$)
- Very fast and robust intrinsic body diode
- Extremely low gate charge and input capacitances

Applications

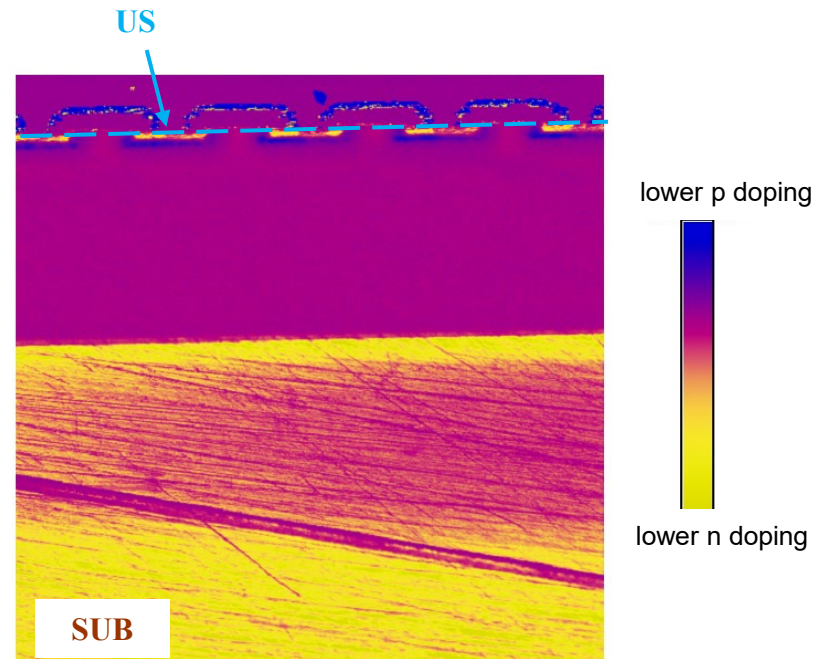
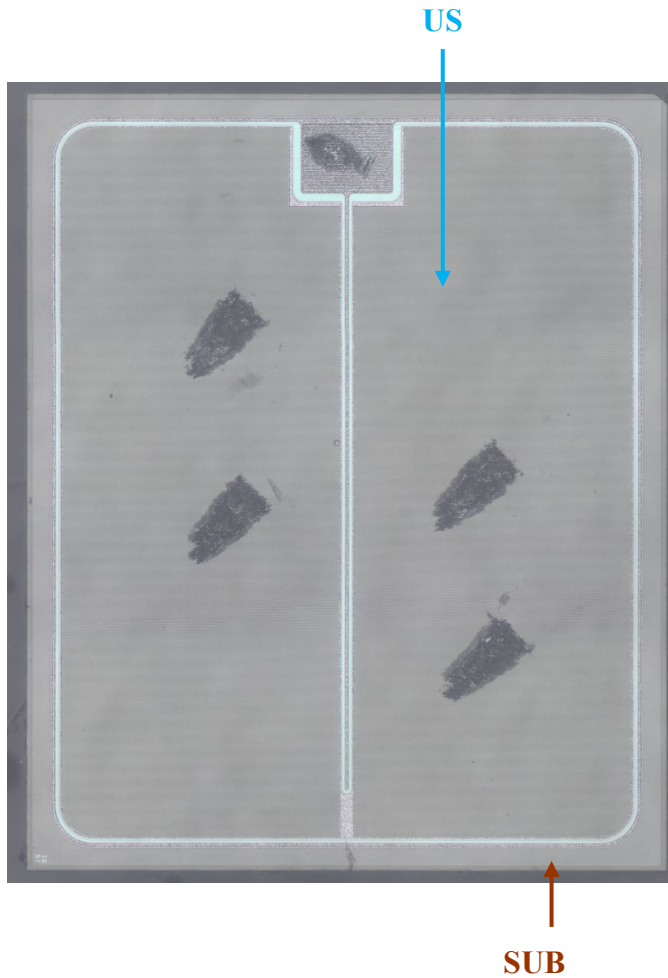
- Charger
- Power supply for renewable energy systems
- High frequency DC-DC converters

Description

This silicon carbide Power MOSFET is produced exploiting the advanced, innovative properties of wide bandgap materials. This results in unsurpassed on-resistance per unit area and very good switching performance almost independent of temperature. The outstanding thermal properties of the SiC material allow designers to use an industry-standard outline with significantly improved thermal capability. These features render the device perfectly suitable for high-efficiency and high power density applications.

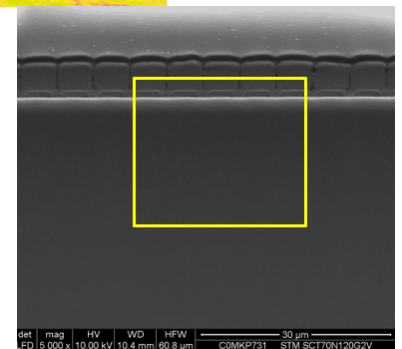
Claim 6

a (SUB) silicon carbide wafer having a substrate body with an (US) upper surface,



SCM Data

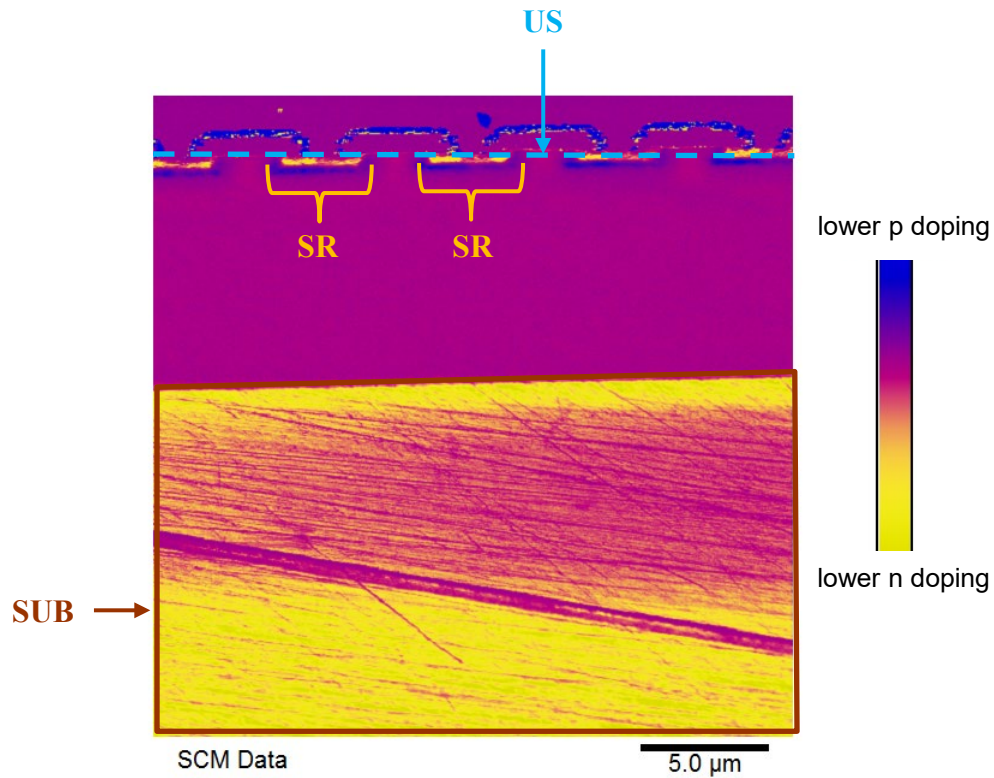
Note: Scanning Capacitance Microscopy (SCM) of the framed area in the Scanning Electron Microscopy (SEM) image.



SEM

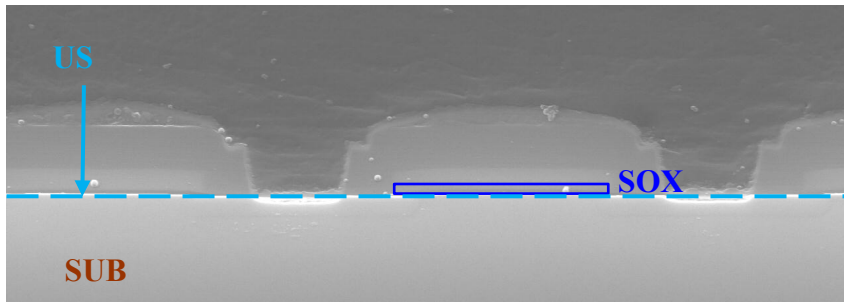
Claim 6

said **(SUB) substrate body** having **(SR) at least one source region** formed **(US) adjacent said upper surface**;

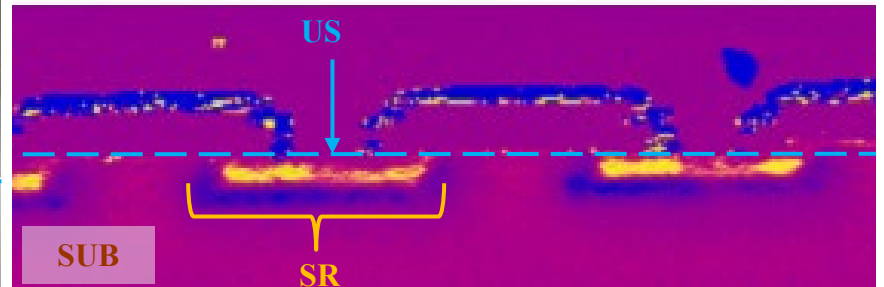


Claim 6

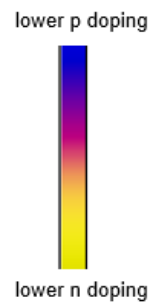
a (SOX) substrate surface oxidation layer on said (US) upper surface of said (SUB) substrate body and (SR) adjacent said source region;



SEM

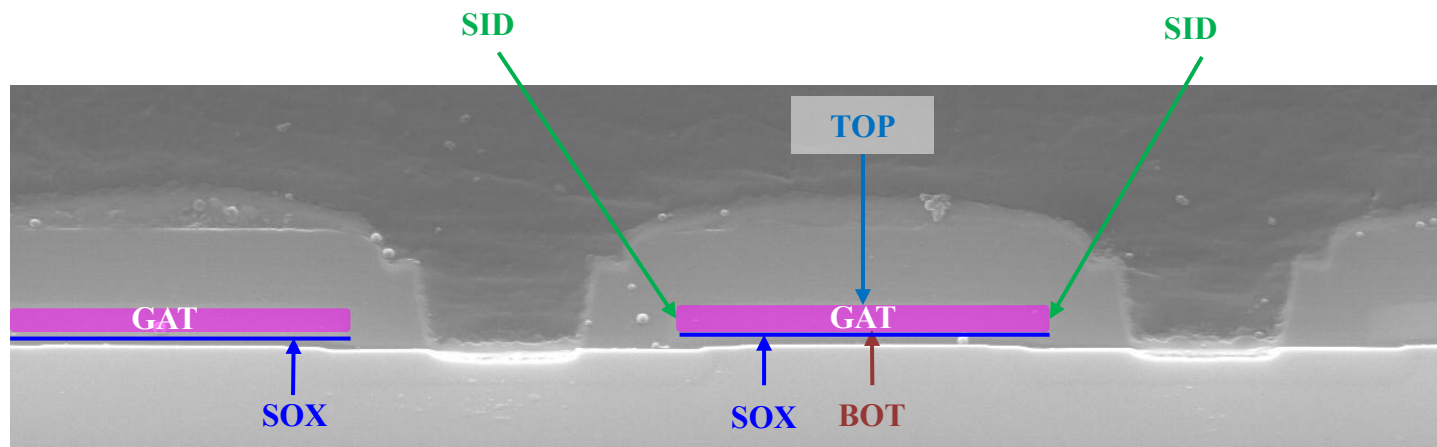


SCM



Claim 6

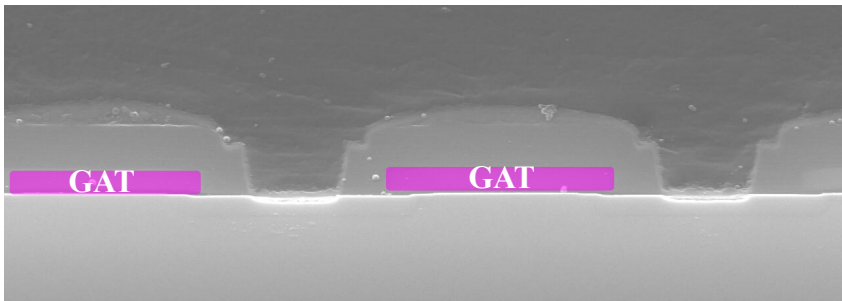
(GAT) at least two polysilicon gates above said (SOX) substrate surface oxidation layer, said (GAT) gates each having a (TOP) top, a (BOT) bottom and (SID) sides,



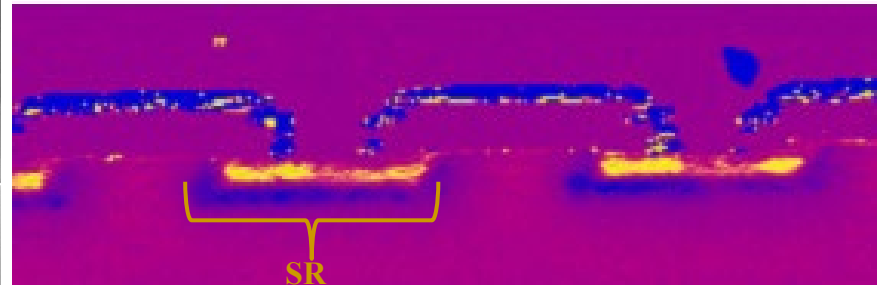
SEM

Claim 6

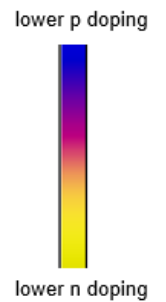
wherein a (SR) first source region of said at least one source region is juxtaposed between (GAT) first and second adjacent gates of said at least two polysilicon gates;



SEM

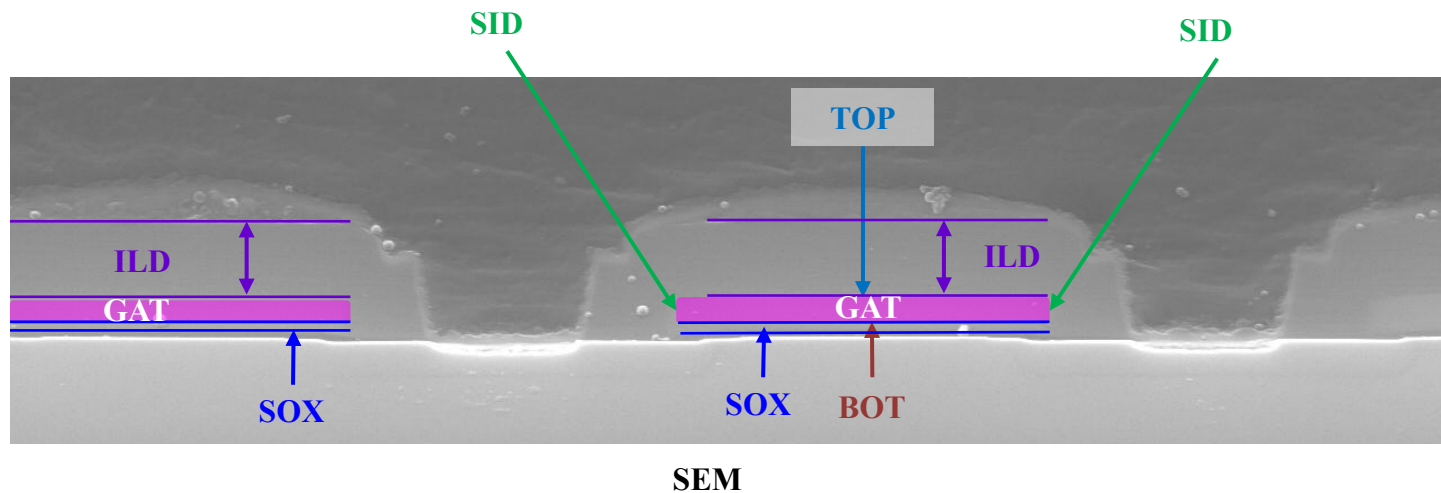


SCM



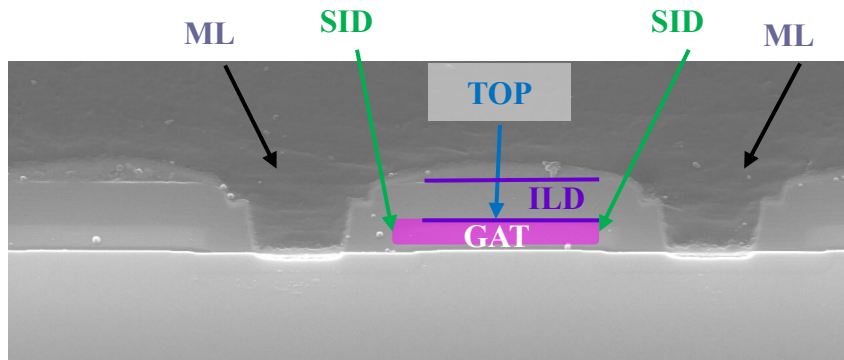
Claim 6

a **(ILD) gate oxide layer**, thicker than said **(SOX) substrate surface oxidation layer**, over said **(TOP) tops** and **(SID) sides** of **(GAT) each of said gates**; and

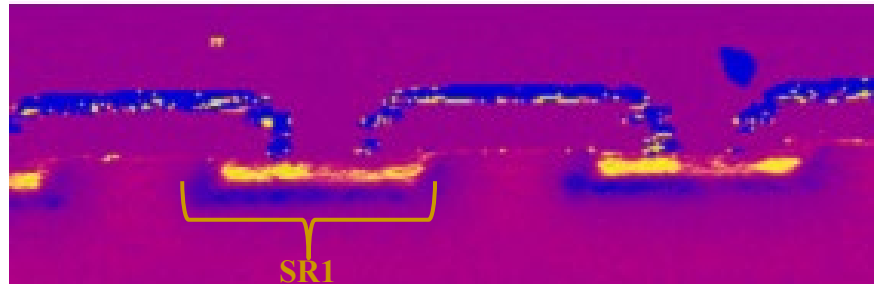


Claim 6

a (ML) material layer over said (SR1) first source region and between said (ILD) gate oxide layers on said (SID) sides of said (GAT) gates, said (ML) material layer comprising one of an oxide and a (ML) metal contact.



SEM

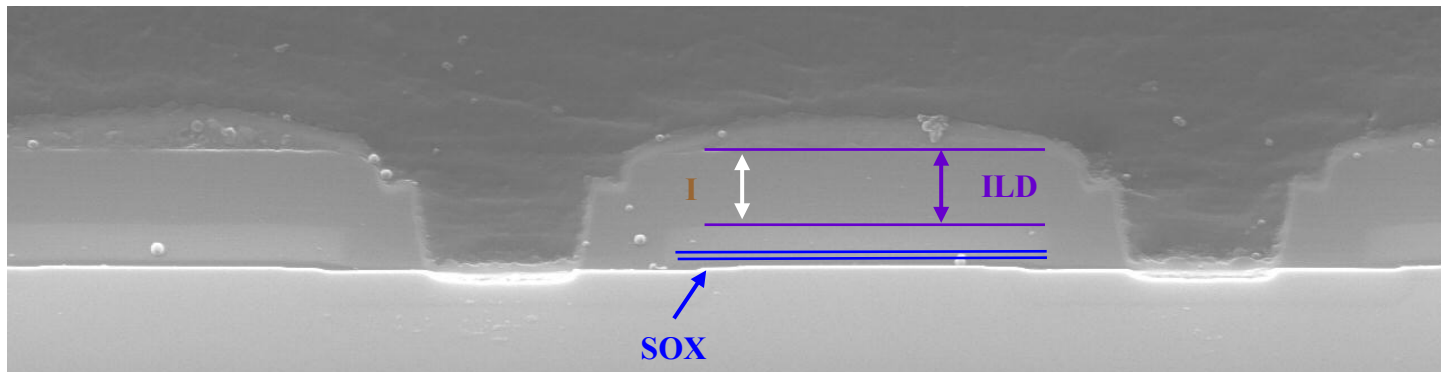


SCM



Claim 7

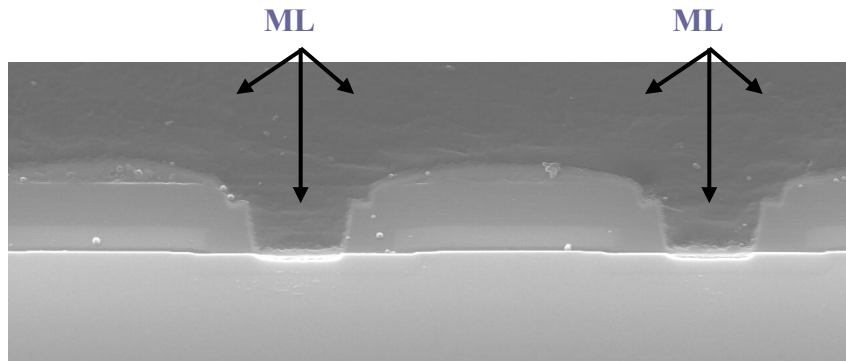
The mosfet structure of claim 6, wherein said **(ILD) gate oxide layer** is more than **(I) eight times thicker** than said **(SOX) substrate surface oxidation layer**.



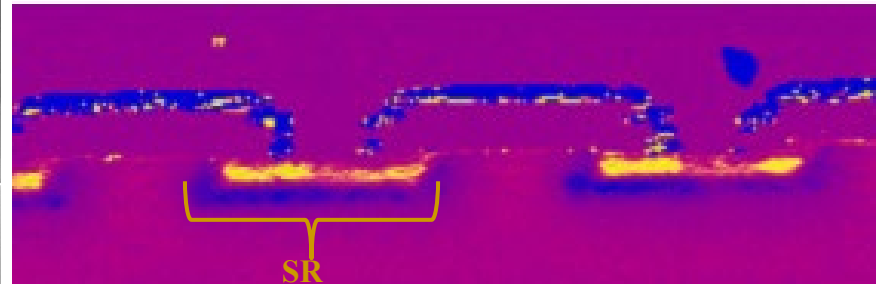
SEM

Claim 10

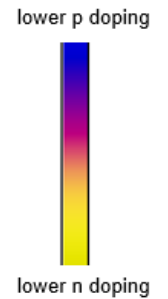
The **MOSFET structure** of claim 6, wherein said **(ML) material layer** is a metal contact layer providing external electrical contact with said at least one **(SR) source region**.



SEM

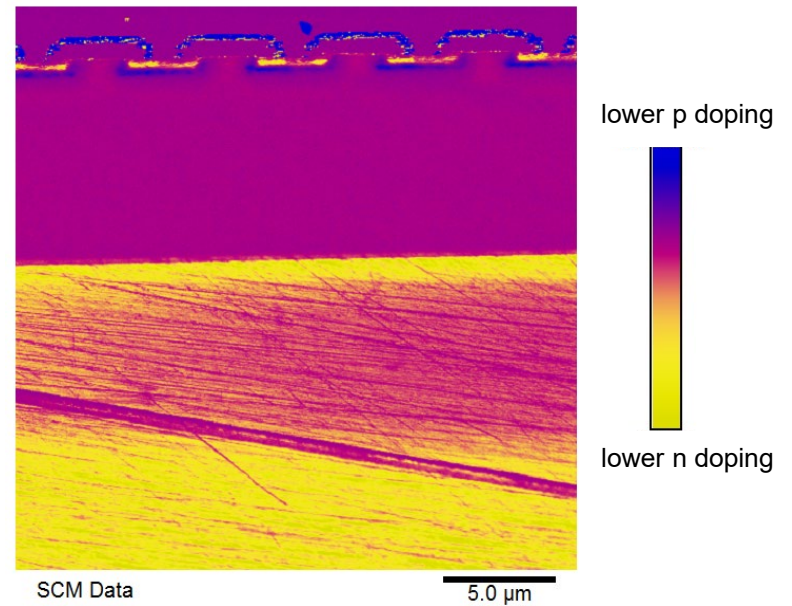
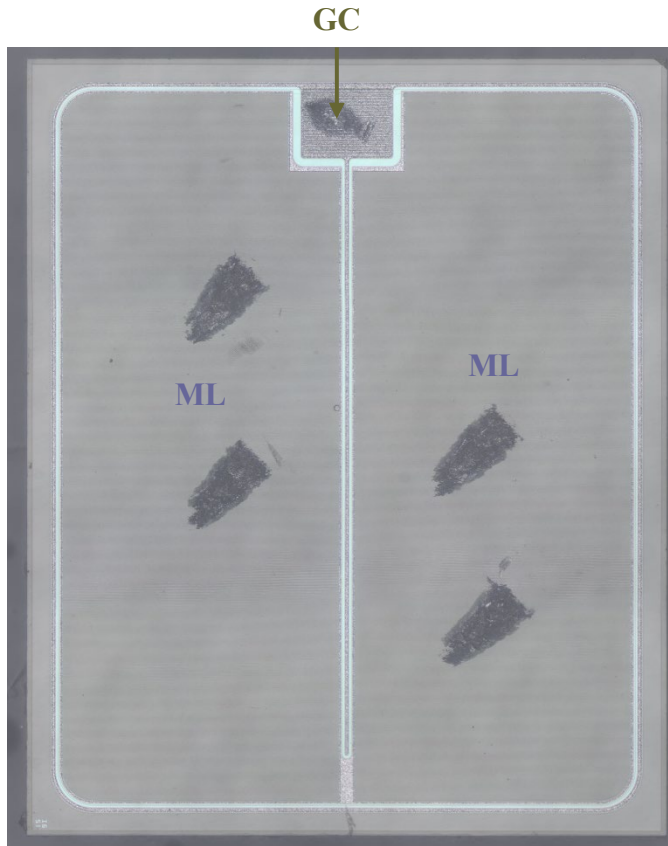


SCM



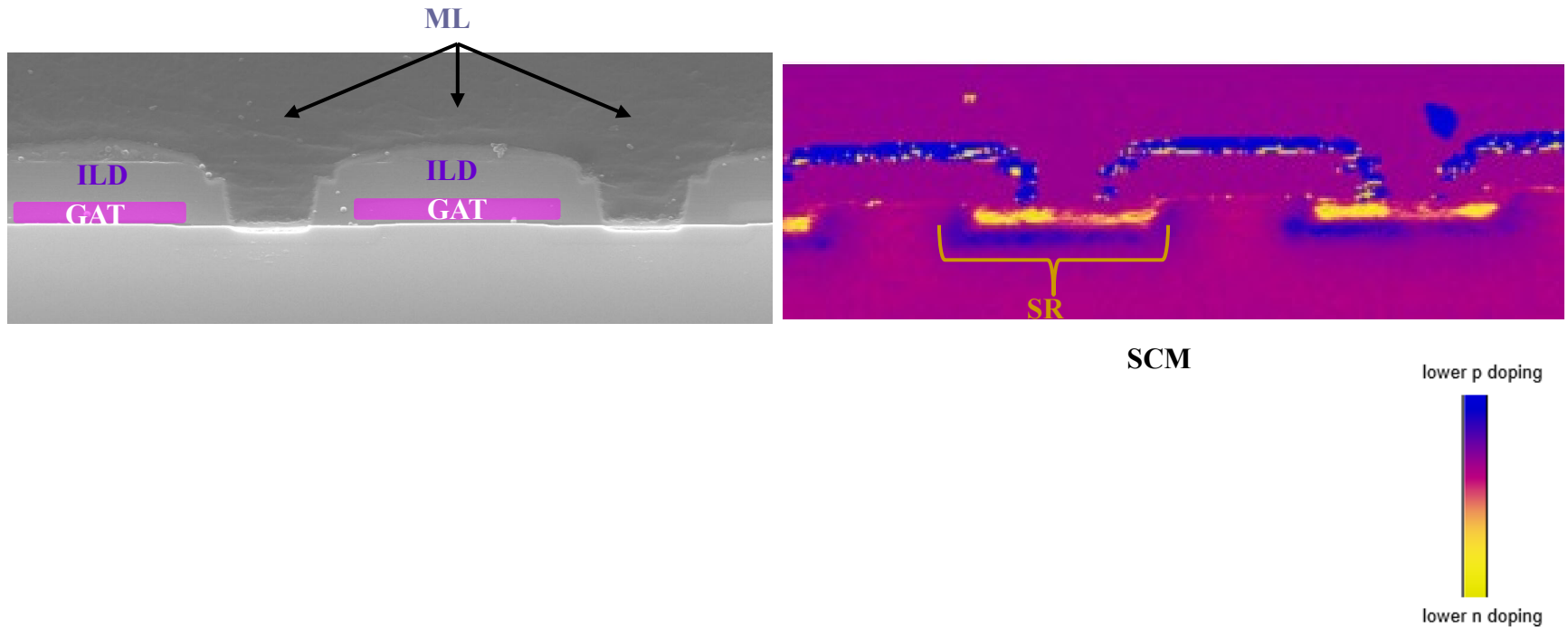
Claim 11

The **MOSFET structure** of claim 10 wherein said **(ML) metal contact layer** extends over substantially the entire MOSFET structure except for at least one **(GC) gate contact access portion**,



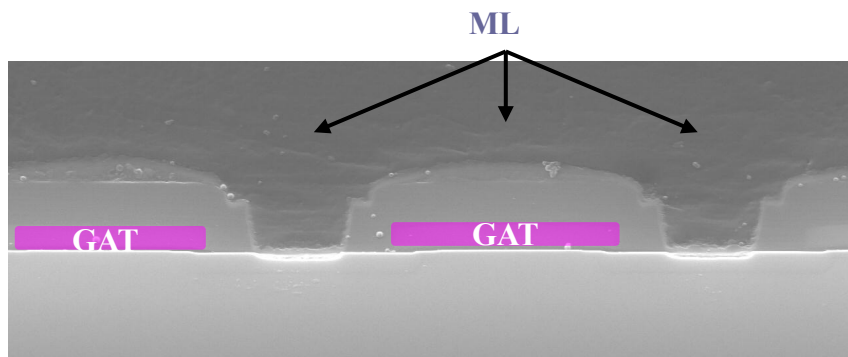
Claim 11

said (ML) metal contact layer being in electrical contact with said **at least one (SR) source region** but **electrically insulated from said at least two (GAT) polysilicon gates by** at least one of said (ILD) gate oxide layer and said substrate surface oxidation layer.

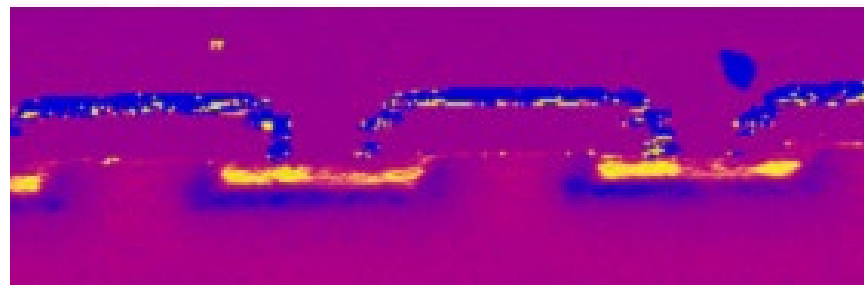


Claim 12

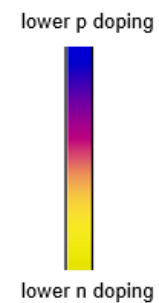
The **MOSFET structure** of claim 10, wherein said **(ML) metal contact layer** extends over said **(GAT) gates** and covers the space between them,



SEM

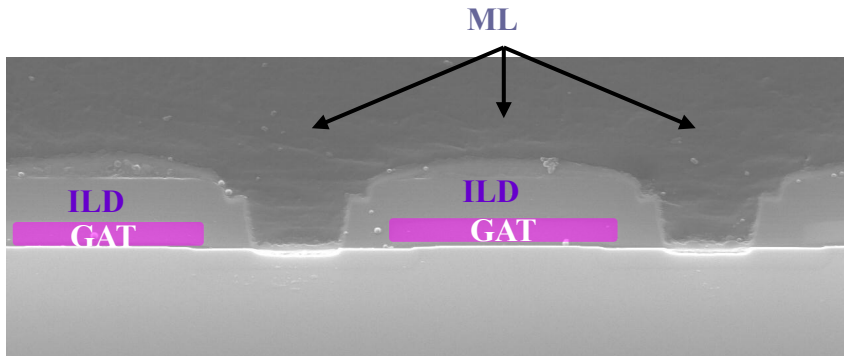


SCM

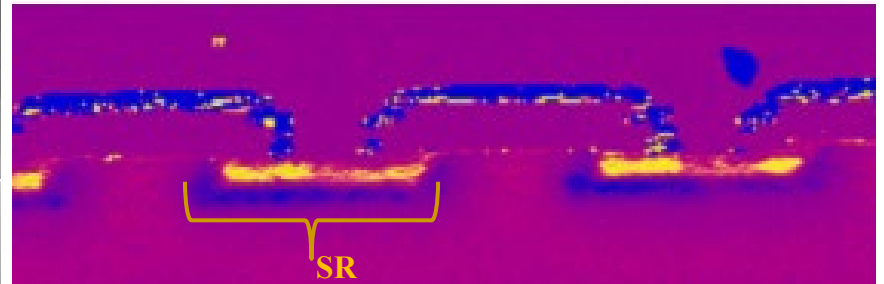


Claim 12

said (ML) metal contact layer being in electrical contact with said at least one (SR) source region but electrically insulated from said (GAT) gates by at least one of said (ILD) gate oxide layer and said substrate surface oxidation layer.



SEM



SCM

